```
=> d l1 1 rn in

L1   ANSWER 1 OF 1  REGISTRY  COPYRIGHT 2001 ACS
RN   7440-21-3  REGISTRY
IN   Silicon (7CI, 8CI, 9CI)

=> d l2 1 rn in

L2   ANSWER 1 OF 1  REGISTRY  COPYRIGHT 2001 ACS
RN   7440-57-5  REGISTRY
IN   Gold (8CI, 9CI)

=> d l3 1 rn in

L3   ANSWER 1 OF 1  REGISTRY  COPYRIGHT 2001 ACS
RN   7440-06-4  REGISTRY
IN   Platinum (8CI, 9CI)

=> d l4 1 rn in

L4   ANSWER 1 OF 1  REGISTRY  COPYRIGHT 2001 ACS
RN   7440-05-3  REGISTRY
IN   Palladium (8CI, 9CI)

=> d l5 1 rn in

L5   ANSWER 1 OF 1  REGISTRY  COPYRIGHT 2001 ACS
RN   7722-84-1  REGISTRY
IN   Hydrogen peroxide (H2O2) (9CI)
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=> file reg

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=> display history full l1-



     FILE 'REGISTRY'
                   E SILICON/CN
L1               1 SEA SILICON/CN
                   E GOLD/CN
L2               1 SEA GOLD/CN
                   E PLATINUM/CN
L3               1 SEA PLATINUM/CN
                   E PALLADIUM/CN
L4               1 SEA PALLADIUM/CN
                   E HYDROGEN PEROXIDE/CN
L5               1 SEA "HYDROGEN PEROXIDE"/CN

     FILE 'LCA'
L6              11 SEA (PERMEA? OR PERFORAT? OR PORO? OR MICROPORO? OR
                   PERVIOUS? OR SEMIPERMEA?)(2A)(L1 OR SILICON OR SI)
L7            7752 SEA FILM? OR THINFILM? OR LAYER? OR OVERLAY? OR OVERLAID?
                    OR LAMIN? OR LAMEL? OR MULTILAYER? OR SHEET? OR LEAF?
                   OR FOIL? OR CLAD? OR COAT? OR TOPCOAT? OR UNDERCOAT? OR
                   OVERCOAT? OR VENEER? OR SHEATH? OR ENVELOP? OR COVER? OR
                   ENCAS? OR ENWRAP? OR OVERSPREAD?
L8            3565 SEA OXIDI? OR OXIDA? OR OXIDN#

     FILE 'REGISTRY'
                   E HYDROFLUORIC ACID/CN
L9               1 SEA "HYDROFLUORIC ACID"/CN

     FILE 'HCA'
L10           8339 SEA (PERMEA? OR PERFORAT? OR PORO? OR MICROPORO? OR
                   PERVIOUS? OR SEMIPERMEA?)(2A)(L1 OR SILICON OR SI)
L11         102980 SEA L9 OR HYDROGEN#(A)(FLUORIDE# OR MONOFLUORIDE#) OR
                   HYDROFLUORIC#(2A)ACID# OR HF
L12          28393 SEA (L2 OR GOLD## OR AU)(2A)L7
L13          20167 SEA (L3 OR PLATINUM# OR PT)(2A)L7
L14          10430 SEA (L4 OR PALLADIUM# OR PD)(2A)L7
L15         139156 SEA L5 OR HYDROGEN#(2A)PEROXIDE# OR H2O2

     FILE 'LCA'
L16            432 SEA ETCH? OR MICROETCH? OR CHASE# OR CHASING# OR ENCHAS?
                   OR ENGRAV? OR MICROENGRAV? OR EMBOSS? OR INCISE# OR
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                INCISING# OR IMPRINT? OR IMPRESS? OR ENCAUSTIC?

     FILE 'HCA'
L17          542 SEA L10 AND L11 AND L16
L18            9 SEA L17 AND (L12 OR L13 OR L14)
L19            3 SEA L18 AND (L8 OR L15)
L20          165 SEA L17 AND (L8 OR L15)
L21           31 SEA L17 AND L15
L22       114123 SEA (L1 OR SILICON OR SI)(2A)(SUBSTRAT? OR SURFACE? OR
                BASE OR BASES OR SUBSTRUCT? OR UNDERSTRUCT? OR UNDERLAY?
                OR FOUNDATION? OR PANE? OR DISK? OR DISC# OR WAFER?)
L23           19 SEA L21 AND L22
L24          148 SEA L17 AND L8
L25           84 SEA L24 AND L22
L26       103246 SEA L2
L27        93427 SEA L3
L28        64010 SEA L4
L29            5 SEA L25 AND (L26 OR L27 OR L28)
L30       156797 SEA METAL####(2A)L7
L31            2 SEA L25 AND L30
L32            2 SEA L24 AND L30
L33          267 SEA L10 AND L22 AND L16 AND L11
L34           84 SEA L33 AND L8
L35           19 SEA L33 AND L15
L36            6 SEA L34 AND (L30 OR L26 OR L27 OR L28)
L37       311754 SEA L1
L38         4109 SEA L37 AND L11 AND L16
L39         1233 SEA L38 AND (L8 OR L15)
L40           20 SEA L39 AND (L12 OR L13 OR L14)
L41           47 SEA L39 AND L30
L42           18 SEA L41 AND L15
L43           32 SEA L41 AND L22
L44           12 SEA L42 AND L22
L45           13 SEA L18 OR L19 OR L29 OR L31 OR L32 OR L36
L46           11 SEA L44 NOT L45
L47            6 SEA L42 NOT (L45 OR L46)
L48           15 SEA (L23 OR L35) NOT (L45 OR L46 OR L47)
L49           17 SEA L40 NOT (L45 OR L46 OR L47 OR L48)
L50           12 SEA L21 NOT (L45 OR L46 OR L47 OR L48 OR L49)

     FILE 'REGISTRY'


=> file hca

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=> d l45 1-13 ibib abs hitind
```

L45 ANSWER 1 OF 13 HCA COPYRIGHT 2001 ACS
ACCESSION NUMBER: 135:350949 HCA
TITLE: Novel **porous silicon** formation technology using internal current Au, Pt generation
AUTHOR(S): Splinter, A.; Sturmann, J.; Benecke, W.
CORPORATE SOURCE: University of Bremen, Institute for Microsensors, -Actuators, and -Systems (IMSAS), Bremen, D-28334, Germany
SOURCE: Mater. Sci. Eng., C (2001), C15(1-2), 109-112
CODEN: MSCEEE; ISSN: 0928-4931
PUBLISHER: Elsevier Science B.V.
DOCUMENT TYPE: Journal
LANGUAGE: English
AB A novel **porous Si** formation technique that combines the advantages of thick layer anodization and electroless stain **etch** is shown. A current generated by a galvanic element of Si and a precious metal on the backside of a **Si wafer** in a **HF**/H2O2/EtOH electrolyte was used to generate **porous Si**. In this case, the Si operates as anode and the metal as cathode for current generation. This current is similar to the external current needed for anodization. Besides the std. **porous Si etch** soln. **HF** (for electrochem. Si dissoln.) and EtOH (to reduce surface tension), an **oxidizing** agent, H2O2, was used to support the **etch** process and to generate a higher **etch** rate. Different kinds of metalization and **etching** solns. were studied and this innovative technol. enables one to generate **porous Si** layers of 10 .mu.m without an external current. The porous structure achieved with this new technol. is comparable with pores generated with anodization.
CC 76-2 (Electric Phenomena)
Section cross-reference(s): 72
ST anodization **etching porous silicon** formation
IT Precious metals
(electrodes; novel **porous silicon** formation technol. using internal current generation)
IT **Etching**
(electroless stain; novel **porous silicon** formation technol. using internal current generation)
IT Anodization
Porous materials
(novel **porous silicon** formation technol. using internal current generation)
IT **7440-06-4**, Platinum, uses **7440-57-5**, Gold, uses
(electrodes; novel **porous silicon** formation technol. using internal current generation)
IT 64-17-5, Ethanol, reactions **7664-39-3**, **Hydrogen**

fluoride, reactions 7722-84-1, Hydrogen peroxide, reactions
(novel **porous silicon** formation technol. using internal current generation)

REFERENCE COUNT: 6

REFERENCE(S):
(1) Archer, R; J Phys Chem Solids 1960, V14, P104 HCA
(2) Ashruf, C; Sens Actuators A 1999, V4, P118
(3) Bartels, O; Proceedings of SPIE Micro/MEMS 1999, V3892, P184 HCA
(4) Bartels, O; SPIE Proceedings Series
(6) Smith, R; J Appl Phys 1992, V71, PR1 HCA
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L45 ANSWER 2 OF 13 HCA COPYRIGHT 2001 ACS

ACCESSION NUMBER: 135:325166 HCA

TITLE: Catalytic Amplification of the Soft Lithographic Patterning of Si. Nonelectrochemical Orthogonal Fabrication of Photoluminescent **Porous Si** Pixel Arrays

AUTHOR(S): Harada, Yoshiko; Li, Xiuling; Bohn, Paul W.; Nuzzo, Ralph G.

CORPORATE SOURCE: Department of Chemistry and the Frederic Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL, 61801, USA

SOURCE: J. Am. Chem. Soc. (2001), 123(36), 8709-8717
CODEN: JACSAT; ISSN: 0002-7863

PUBLISHER: American Chemical Society

DOCUMENT TYPE: Journal

LANGUAGE: English

AB Photoluminescent, **porous silicon** pixel arrays were fabricated via a Pt-promoted wet **etching** of p-type Si(100) using EtOH/**HF**/**H2O2** soln. in 1:1:1 ratio. The pixels were fabricated with micrometer-scale design rules on a **silicon substrate** that had been modified with an octadecyltrichlorosilane (OTS) monolayer patterned using microcontact printing. The printed OTS layer serves as an orthogonal resist template for the deposition of a Pt(0) complex, which preferentially deposits metal species in areas not covered with OTS. The Pt centers generate a localized **oxidative** dissoln. process that pits the Si in the **Pt-coated** regions, resulting in the formation of a **porous silicon** microstructure that luminesces around 580 nm upon illumination with a UV source. SEM and fluorescence microscopy images of the fabricated **porous silicon** structures showed that features in the size range of .apprx.10-150 .mu.m, and possibly smaller, can be generated by this catalytically amplified soft lithog. patterning method. Importantly, the OTS acts as an **etch** mask, so that, even with significant hole transport, **etching** is confined to areas **coated** with the **Pt**(0) complex.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): 73, 76
ST **porous** photoluminescent **silicon** fabrication catalytically amplified soft lithog patterning; pixel array **porous** photoluminescent **silicon** nonelectrochem lithog patterning fabrication
IT **Etching**
Lithography
Luminescence
(fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
IT Polysiloxanes, processes
(fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
IT Porous materials
(microporous; fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
IT 30110-75-9, Divinyltetramethyldisiloxane
(**etching** aid; fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
IT **7664-39-3**, **Hydrofluoric acid**, processes
7722-84-1, **Hydrogen peroxide**, processes
(**etching** soln.; fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
IT **7440-06-4**, Platinum, processes
(fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
IT 112-04-9, Octadecyltrichlorosilane 9016-00-6, Poly(dimethylsiloxane) 31900-57-9, Poly(dimethylsiloxane)
(fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
IT 7440-21-3, Silicon, properties
(fabrication of photoluminescent **porous silicon** pixel arrays using catalytically amplified soft lithog. patterning)
REFERENCE COUNT: 46
REFERENCE(S):
(1) Bao, X; Appl Phys Lett 1993, V63, P2246 HCA
(2) Beale, M; Appl Phys Lett 1985, V46, P86 HCA
(3) Beale, M; J Cryst Growth 1985, V73, P622 HCA
(4) Beale, M; J Cryst Growth 1986, V75, P408 HCA
(5) Canham, L; Appl Phys Lett 1990, V57, P1046 HCA
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L45 ANSWER 3 OF 13 HCA COPYRIGHT 2001 ACS
ACCESSION NUMBER: 135:186101 HCA
TITLE: Study on hydrogen reactivity with surface chemical species of nanocrystalline **porous silicon**
AUTHOR(S): Tuyen, L. T. T.; Tam, N. T. T.; Quang, N. H.; Nghia, N. X.; Khang, D. D.; Khoi, P. H.
CORPORATE SOURCE: NCST, Institute of Materials Science, Hanoi, Cau giay District, Vietnam
SOURCE: Mater. Sci. Eng., C (2001), C15(1-2), 133-135
CODEN: MSCEEE; ISSN: 0928-4931
PUBLISHER: Elsevier Science B.V.
DOCUMENT TYPE: Journal
LANGUAGE: English
AB The nanocryst. **porous silicon** was prepd. by the electrochem. **etching** of Si in a **HF** soln. A semi-transparent **palladium layer** was thermally deposited on its surface. Micro-Raman spectra were recorded in air and in the presence of hydrogen. Different Si-HX stretching and wagging vibrational modes, a Si-H stretching mode modified by the presence of three oxygen atoms in the Si backbonds (O3-Si-H unit) and a Si-O-Si vibration were readily revealed. Their behavior under laser irradn. and towards the hydrogen atoms dissocd. from hydrogen mols. by palladium is reported.
CC 67-3 (Catalysis, Reaction Kinetics, and Inorganic Reaction Mechanisms)
Section cross-reference(s): 66
ST hydrogen reactivity surface chem species nanocryst **porous silicon**
IT Dissociation catalysts
Nanocrystals
Surface reaction
(study on hydrogen reactivity with surface chem. species of nanocryst. **porous silicon**)
IT 7440-05-3, Palladium, uses
(study on hydrogen reactivity with surface chem. species of nanocryst. **porous silicon**)
IT 1333-74-0, Hydrogen, reactions 7440-21-3, Silicon, reactions
(study on hydrogen reactivity with surface chem. species of nanocryst. **porous silicon**)
REFERENCE COUNT: 9
REFERENCE(S): (3) Hill, N; Journal of Electronic Materials 1996, V25, P269 HCA
(5) Khoi, P; Journal of Raman Spectroscopy 1999, V30, P385 HCA
(7) Lundstroem, I; Sensors and Actuators 1981, V1, P403 HCA
(8) Quang, N; Technical digest of the Seventh International Meeting on Chemical Sensors 1998, P663 HCA
(9) Theiss, W; Surface Science Report 1997, V29, P91 HCA

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L45 ANSWER 4 OF 13 HCA COPYRIGHT 2001 ACS
ACCESSION NUMBER: 135:27293 HCA
TITLE: Novel **porous silicon** formation without external contact
AUTHOR(S): Splinter, Alexandra; Stuermann, Joerg; Benecke, Wolfgang
CORPORATE SOURCE: Institute for Microsensors, Actuators and, Systems (IMSAS), University of Bremen, Bremen, D-28334, Germany
SOURCE: Proc. SPIE-Int. Soc. Opt. Eng. (2000), 4174(Micromachining and Microfabrication Process Technology VI), 398-405
CODEN: PSISDG; ISSN: 0277-786X
PUBLISHER: SPIE-The International Society for Optical Engineering
DOCUMENT TYPE: Journal
LANGUAGE: English

AB Presently 2 **porous Si** (PS) formation technologies are published: the anodization into an electrochem. cell and stain **etch** without external current into a **HF**/HNO3 soln. For anodization an external current is necessary to achieve PS thicknesses .ltoreq.100 .mu.m. Stain **etch** is an electroless process, and the porous layer thickness sis limited to a few micrometers. A novel PS formation technique that combines the advantages of thick layer anodization and electroless stain **etch** will be shown. A current generated by a galvanic element of Si and a precious metal on the backside of a **Si wafer** in a **HF** /H2O2/EtOH electrolyte is utilized to generate PS. In this case the Si operates as anode and the metal as cathode for current generation. This current is similar to the external current needed for anodization. Beside the std. PS **etch** soln. **HF** and EtOH to **oxidizing** agent H2O2 is used to support the **etch** process and to generate a higher **etch** rate. **Etch** rate control is given by concn. of **etching** soln. and metalization. Different kinds of metalizations and **etching** solns. were investigated. This novel technol. enables to generate stable PS layers of e.g. 80 .mu.m within 10 min without an external current. This can be the 1st efficient way for PS batch processing. Detailed process parameters and characterization will be presented.

CC 76-2 (Electric Phenomena)
Section cross-reference(s): 72

ST **porous silicon** fabrication electrochem **etching** hydrogen peroxide **hydrofluoric acid**

IT **Etching**
(electrochem.; **porous silicon** fabrication by electrochem. **etching** without external contact)

IT **Porosity**

(**porous silicon** fabrication by electrochem.
etching without external contact)
IT **7440-57-5**, Gold, uses
(**porous silicon** fabrication by electrochem.
etching without external contact using Au backside
contact)
IT 64-17-5, Ethanol, uses **7664-39-3**, **Hydrofluoric acid**, uses 7722-84-1, Hydrogen peroxide, uses
(**porous silicon** fabrication by electrochem.
etching without external contact using **HF**
/H2O2/EtOH electrolyte)
IT **7440-06-4**, Platinum, uses
(**porous silicon** fabrication by electrochem.
etching without external contact using Pt backside
contact)
IT **7440-21-3**, **Silicon**, properties
(**porous**; **porous silicon** fabrication
by electrochem. **etching** without external contact)
REFERENCE COUNT: 7
REFERENCE(S):
(1) Archer, R; J Phys, "Stain films on silicon", Chem Solids 1960, V14, P104 HCA
(2) Ashruf, C; Sensors and Actuators A 1999, V4, P118
(3) Bartels, O; Proceedings of SPIE Micro/MEMS '99, Device and Process Technologies for MEMS and Microelectronics 1999, V3892, P184 HCA
(4) Canham, L; "Properties of porous silicon", emis datareviews series no 18 1997
(7) Smith, R; J Appl Phys 1992, V71, PR1 HCA
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L45 ANSWER 5 OF 13 HCA COPYRIGHT 2001 ACS
ACCESSION NUMBER: 134:48949 HCA
TITLE: Metal-assisted chemical **etching** in **HF/H2O2** produces **porous silicon**
AUTHOR(S): Li, X.; Bohn, P. W.
CORPORATE SOURCE: Materials Research Laboratory, Beckman Institute and Department of Chemistry, University of Illinois at Urbana-Champaign, Urbana, IL, 61801, USA
SOURCE: Appl. Phys. Lett. (2000), 77(16), 2572-2574
CODEN: APPLAB; ISSN: 0003-6951
PUBLISHER: American Institute of Physics
DOCUMENT TYPE: Journal
LANGUAGE: English
AB A simple and effective method is presented for producing light-emitting **porous Si** (PSi). A thin (d < 10 nm) **layer** of **Au**, **Pt**, or Au/Pd is deposited on the (100) Si surface prior to immersion in a soln. of **HF** and **H2O2**. Depending on the type of metal

deposited and Si doping type and doping level, PSi with different morphologies and light-emitting properties is produced. PSi prodn. occurs on the time scale of seconds, without elec. current, in the dark, on both p- and n-type Si. Thin metal coatings facilitate the **etching** in **HF** and **H2O2**, and of the metals investigated, Pt yields the fastest **etch** rates and produces PSi with the most intense luminescence. A reaction scheme involving local coupling of redox reactions with the metal is proposed to explain the metal-assisted **etching** process. The observation that some metal remains on the PSi surface after **etching** raises the possibility of fabricating in situ PSi contacts.

CC 73-12 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76

ST **porous silicon** luminescence metal assisted **etching**

IT **Etching**
Luminescence
(**porous Si** prodn. by metal-assisted chem. **etching** in **HF**/**H2O2** and its luminescence)

IT 7440-06-4, Platinum, uses 7440-57-5, Gold, uses 11106-95-9
(**porous Si** prodn. by metal-assisted chem. **etching** in **HF**/**H2O2** and its luminescence)

IT **7664-39-3**, **Hydrogen fluoride**, uses
7722-84-1, **Hydrogen peroxide**, uses
(**porous Si** prodn. by metal-assisted chem. **etching** in **HF**/**H2O2** and its luminescence)

IT **7440-21-3**, **Silicon**, properties
(**porous Si** prodn. by metal-assisted chem. **etching** in **HF**/**H2O2** and its luminescence)

REFERENCE COUNT: 13

REFERENCE(S):
(1) Brus, L; J Phys Chem 1994, V98, P3575 HCA
(2) Canham, L; Adv Mater 1995, V7, P1033 HCA
(3) Canham, L; Appl Phys Lett 1990, V57, P1046 HCA
(4) Cullis, A; J Appl Phys 1997, V82, P909 HCA
(5) Koker, L; Phys Chem Chem Phys 2000, V2, P277 HCA
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L45 ANSWER 6 OF 13 HCA

ACCESSION NUMBER: 132:243655 HCA

TITLE: **Porous silicon** micromachining to position optical fibers in silicon integrated optical circuits

AUTHOR(S): Joubert, P.; Guendouz, M.; Pedrono, N.; Charrier, J.

CORPORATE SOURCE: Groupe de Microelectronique et Visualisation, Universite de Rennes 1, Lannion, 22302, Fr.
SOURCE: J. Porous Mater. (2000), 7(1/2/3), 227-231
CODEN: JPMAFX; ISSN: 1380-2224
PUBLISHER: Kluwer Academic Publishers
DOCUMENT TYPE: Journal
LANGUAGE: English

AB Low-loss optical fiber connections require deep grooves **etched** in Si substrate for accurate fiber positioning. As shown these grooves can be obtained by using localized formation of **porous Si** on patterned substrates. Cr-**Au** masking **layer** with a duration in **HF** soln. longer than 30 min was used to fabricate grooves with a depth >75 .mu.m. N+-type Si provides grooves with a pseudo-V shape which is compatible with accurate fiber alignment. By using this technol., arrays of optical fibers are positioned with an accuracy >1 .mu.m.

CC 73-11 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76

ST **porous silicon** micromachining optical fiber integrated circuit

IT **Etching**
(electrochem.; **porous silicon** micromachining to position optical fibers in silicon integrated optical circuits using **HF** soln.)

IT Anodization
(localized; **porous silicon** micromachining to position optical fibers in silicon integrated optical circuits using **HF** soln.)

IT Micromachining
Optical fibers
Optical integrated circuits
(**porous silicon** micromachining to position optical fibers in silicon integrated optical circuits using **HF** soln.)

IT 7440-47-3, Chromium, uses 7440-57-5, Gold, uses
(mask; **porous silicon** micromachining to position optical fibers in silicon integrated optical circuits)

IT **7664-39-3**, **Hydrogen fluoride**, processes
(**porous silicon** micromachining to position optical fibers in silicon integrated optical circuits using **HF** soln.)

IT **7440-21-3**, **Silicon**, properties
(**porous**; **porous silicon** micromachining to position optical fibers in silicon integrated optical circuits)

REFERENCE COUNT: 12

REFERENCE(S):
(1) Bean, K; IEEE Trans Electron Devices 1978, VED-25, P1185 HCA
(2) Bean, K; IEEE Trans Electron Devices 1978, VED-25, P1185 HCA
(3) Guendouz, M; Electron Lett 1997, V33, P1695

HCA
(4) Guendouz, M; Materials and Devices for Si-Based Optoelectronics, Mat Res Soc Symp Proc 1998, V486, P373 HCA
(7) Lee, M; Jpn J Appl Phys 1996, V35, PL865 HCA
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L45 ANSWER 7 OF 13 HCA
ACCESSION NUMBER: 132:215710 HCA
TITLE: Preparation of masking layers in production of **porous silicon** by **etching**
INVENTOR(S): Frey, Wilhelm; Artmann, Hans; Splinter, Alexandra
PATENT ASSIGNEE(S): Robert Bosch G.m.b.H., Germany
SOURCE: Ger. Offen., 6 pp.
CODEN: GWXXBX
DOCUMENT TYPE: Patent
LANGUAGE: German
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 19842105	A1	20000316	DE 1998-19842105	19980915

AB Formation of masking multilayers on a **Si** layer or **wafer** involves (1) formation of a SiO2 layer 20-2,000 nm thick by thermal **oxidn**. and (2) formation of an adherent layer (e.g., Cr) 10-1,000 nm thick and/or a protective **layer** (e.g., **Au**) 10-1,000 nm thick by evapn., sputtering, or chem. deposition on the SiO2 layer. **Porous Si** is prepd. by using an electrochem. procedure, esp. **HF** electrolytes. The **porous Si** is suitable for optical devices, chem. sensors, and surface micromechanics.

IC ICM C23C028-00
ICS C23C030-00; C25F003-02

CC 76-3 (Electric Phenomena)

ST masking layer prepn silicon **etching**; sensor **porous silicon** prepn; optical device **porous silicon** prepn

IT Noble **metals**
(in masking **layers** in prodn. of **porous silicon** by **etching**)

IT **Etching**
(prepn. of masking layers in prodn. of **porous silicon** by)

IT Optical sensors
Sensors
(prepn. of masking layers in prodn. of **porous silicon** for)

IT 409-21-2, Silicon carbide, uses 7439-96-5, Manganese, uses 7439-98-7, Molybdenum, uses 7440-02-0, Nickel, uses 7440-25-7,

Tantalum, uses 7440-32-6, Titanium, uses 7440-47-3, Chromium, uses 7440-48-4, Cobalt, uses 7440-50-8, Copper, uses **7440-57-5**, Gold, uses 7440-62-2, Vanadium, uses 7440-66-6, Zinc, uses 7631-86-9, Silica, uses 11105-01-4, Silicon oxynitride 12033-89-5, Silicon nitride, uses 39345-87-4, Silicon oxycarbide
(in masking layers in prodn. of **porous silicon** by **etching**)

IT 7440-21-3P, Silicon, processes
(prepn. of masking layers in prodn. of **porous silicon** by **etching**)

L45 ANSWER 8 OF 13 HCA COPYRIGHT 2001 ACS
ACCESSION NUMBER: 130:189121 HCA
TITLE: Fabrication of integrated micromirror from **porous silicon**
INVENTOR(S): Laermer, Franz; Frey, Wilhelm; Artmann, Hans
PATENT ASSIGNEE(S): Bosch, Robert, G.m.b.H., Germany
SOURCE: Ger. Offen., 10 pp.
CODEN: GWXXBX
DOCUMENT TYPE: Patent
LANGUAGE: German
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 19738607	A1	19990311	DE 1997-19738607	19970904

AB An inexpensive and simple method is described for prepg. an integrated laser micromirror using **porous silicon** . The method consists of anisotropic **etching** the **Si wafer** in KOH, electrochem. **etching** the silicon in a mixt. of **HF** and ethanol, anodizing, and thermally **oxidizing**.

IC ICM H01L049-00
ICS G02B006-132; G02B006-293; G02B006-42; G03F007-00

CC 73-10 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)

ST **porous silicon** micromirror fabrication

IT Laser mirrors
Porous materials
Semiconductor device fabrication
(fabrication of integrated micromirror from **porous silicon**)

IT Anisotropic **etching**
Anodizing
Chemical vapor deposition
Electrochemical **etching**
Ion implantation
Photolithography
Thermal **oxidation**
(in fabrication of integrated micromirror from **porous**

silicon)

IT 7440-21-3, Silicon, uses
(fabrication of integrated micromirror from **porous silicon**)

IT **7440-06-4**, Platinum, uses 12033-89-5, Silicon nitride, uses
(in fabrication of integrated micromirror from **porous silicon**)

IT 7631-86-9P, Silica, uses
(in fabrication of integrated micromirror from **porous silicon**)

IT 64-17-5, Ethanol, uses
(in fabrication of integrated micromirror from **porous silicon**)

IT 1310-58-3, Potassium hydroxide (KOH), reactions **7664-39-3**, **Hydrogen fluoride**, reactions
(in fabrication of integrated micromirror from **porous silicon**)

L45 ANSWER 9 OF 13 HCA COPYRIGHT 2001 ACS

ACCESSION NUMBER: 127:26972 HCA

TITLE: Improvement in Photovoltage and Stability of **Porous** n-**Si** Electrodes **Coated** with **Platinum** by Regulation of the Thickness of Nanoporous Layers

AUTHOR(S): Kawakami, Kazuyuki; Fujii, Takashi; Yae, Shinji; Nakato, Yoshihiro

CORPORATE SOURCE: Graduate School of Engineering Science, Osaka University, Osaka, 560, Japan

SOURCE: J. Phys. Chem. B (1997), 101(23), 4508-4513
CODEN: JPCBFK; ISSN: 1089-5647

PUBLISHER: American Chemical Society

DOCUMENT TYPE: Journal

LANGUAGE: English

AB **Porous** n-**Si** electrodes, prepd. by photo-**etching** in **HF** under appropriate conditions, have macroporous layers at the surface, consisting of micrometer-sized pores and Si pillars. The wall and top of the Si pillars are further covered with 0.2-0.5-.mu.m-thick nano porous layers having nm-sized pores. The nano porous layer can be thinned by immersion in **HF**. The solar cell characteristics (open-circuit photo-voltage VOC, fill factor, and stability) for the **porous** n-**Si** electrodes with **Pt coating** in 8.6M HBr/0.05 M Br2 were improved by thinning the nano-porous layer to an appropriate thickness, although the electrodes with no nano-porous layers gave only poor characteristics. The max. solar energy conversion efficiency of 14% (VOC 0.575 V, jSC 34.7 mA cm-2, and fill factor 0.701) was obtained, which is 1 of the highest for n-Si photo-electrochem. solar cells. A mechanism for the generation of high VOC's as well as high fill factors in **porous Si**-based photo-electrochem. solar cells is discussed including a possibility of a low

resistivity of the nano-porous layer for hole transport.
CC 76-5 (Electric Phenomena)
Section cross-reference(s): 52
ST photo voltage stability **porous silicon** electrode; **platinum** thickness nanoporous **film** electrode coated
IT Porous materials
(films, nanoporous; improvement in photovoltage and stability of **porous** n-**Si** electrodes **coated** with **platinum** by regulation of thickness of nanoporous layers)
IT Microstructure
Photovoltage
Porous electrodes
Solar cells
(improvement in photovoltage and stability of **porous** n-**Si** electrodes **coated** with **platinum** by regulation of thickness of nanoporous layers)
IT Films
(porous, nanoporous; improvement in photovoltage and stability of **porous** n-**Si** electrodes **coated** with **platinum** by regulation of thickness of nanoporous layers)
IT 7440-06-4, Platinum, uses 7440-21-3, Silicon, uses
(improvement in photovoltage and stability of **porous** n-**Si** electrodes **coated** with **platinum** by regulation of thickness of nanoporous layers)

L45 ANSWER 10 OF 13 HCA COPYRIGHT 2001 ACS
ACCESSION NUMBER: 124:244911 HCA
TITLE: Enhanced photoelectrochemical behavior of **gold-coated porous** n-**Si** electrochemically modified with polyaniline
AUTHOR(S): Park, Soo-Jin; Chae, Won-Seok; Kim, Kang-Jin
CORPORATE SOURCE: Department Chemistry, Korea University, Seoul, 136-701, S. Korea
SOURCE: Anal. Sci. Technol. (1995), 8(4), 637-42
CODEN: ASCTET; ISSN: 1225-0163
DOCUMENT TYPE: Journal
LANGUAGE: English
AB The presence of a **porous Si** layer (PSL) formed on the surface of cryst. silicon by electrochem. **etching** in **HF** soln. is found to enhance the stability of n-**Si** photoanodes, but **porous** n-**Si** thus formed is still liable to corrode upon exposure to excitation light. To improve the stability of the **porous** n-**Si** electrodes and to reduce the photo-induced corrosion, the authors have examd. the PEC behavior of **porous** n-**Si** modified with polyaniline (PANI) and 3 nm thick **layer** of **Au**. Comparisons were made between Au/PSL and PANI/Au/PSL photoelectrodes.
CC 72-4 (Electrochemistry)
Section cross-reference(s): 66, 76

ST photoelectrochem behavior **gold coated** silicon
polyaniline
IT Photoconductivity and Photoconduction
Photovoltaic effect
(of **gold-coated porous** n-**Si**
electrochem. modified with polyaniline in sulfuric acid in
presence of redox couple)
IT Electrodes
(photoelectrochem., of **gold-coated**
porous n-**Si** electrochem. modified with
polyaniline)
IT 7440-21-3, Silicon, uses 7440-57-5, Gold, uses 25233-30-1,
Polyaniline
(enhanced photoelectrochem. behavior of **gold-**
coated porous n-**Si** electrochem.
modified with polyaniline)
IT 102-54-5, Ferrocene 106-51-4, Quinone, properties 123-31-9,
Hydroquinone, properties 7439-89-6, Iron, properties 7440-50-8,
Copper, properties 12125-80-3, Ferrocenium 13408-62-3,
Ferricyanide 13408-63-4, Ferrocyanide 14900-04-0, Iodide i31-
15454-31-6, Iodate io31- 20461-54-5, Iodide, properties
(photoelectrochem. properties of **gold-coated**
porous n-**Si** electrochem. modified with
polyaniline in sulfuric acid in presence of)
IT 7664-93-9, Sulfuric acid, properties
(photoelectrochem. properties of **gold-coated**
porous n-**Si** electrochem. modified with
polyaniline in sulfuric acid in presence of redox couple)

L45 ANSWER 11 OF 13 HCA COPYRIGHT 2001 ACS
ACCESSION NUMBER: 120:203384 HCA
TITLE: Spectroscopic investigation of electroluminescent **porous silicon**
AUTHOR(S): Pavesi, L.; Ceschini, M.; Mariotto, G.; Zanghellini, E.; Bisi, O.; Anderle, M.; Calliari, L.; Fedrizzi, M.; Fedrizzi, L.
CORPORATE SOURCE: Dip. Fis., Univ. Trento, Povo, I-38050, Italy
SOURCE: J. Appl. Phys. (1994), 75(2), 1118-26
CODEN: JAPIAU; ISSN: 0021-8979
DOCUMENT TYPE: Journal
LANGUAGE: English
AB Light-emitting **porous Si** films were obtained by anodic **etching** p-type Si samples in a **HF**-EtOH soln. **Porous Si** samples efficiently luminesce at room temp. in the visible region. A degrdn. of the luminescence intensity with time is obsd. Micro-Raman spectroscopy of free-standing **porous Si** layers indicates phonon confinements as well as a strong laser heating effects. The surface chem. compn. and the effect of electron-beam irradn. was studied through Auger spectroscopy. The Si LVV Auger transition dominates the spectrum, even in aged samples. The Si line shape gives

evidence of a covalent bond between the **porous Si** surface atoms and some adsorbed species. A prolonged electron irradn. results in a strong variation of the surface chem. compn., with an anomalous C accumulation. **Au** thin **films** were deposited on the **porous Si** surface to form metal-semiconductor junctions. Schottky diodes with large rectifying ratio, ideality factor, and series resistance are obtained. When the junction is forward biased, electroluminescence is obsd. Electroluminescence degrades with time while the current does not. When the junction is reverse biased a significant photocurrent is obtained. The results are discussed in the framework of the surface state emission model for the luminescence.

CC 73-5 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 79

ST **porous silicon** electroluminescence Schottky diode; gold **porous silicon** electroluminescence Schottky diode; carbon detn **porous silicon** Auger

IT Luminescence
(of **porous silicon**)

IT Electroluminescent devices
(**porous silicon**/gold Schottky diode)

IT Diodes
(Schottky, **porous silicon**/gold)

IT 7440-57-5, Gold, uses
(Schottky diodes from **porous silicon** and)

IT 7440-44-0, Carbon, analysis
(detn. of, in **porous silicon** by electron-beam Auger spectroscopy)

IT **7440-21-3**, **Silicon**, properties
(**porous**, luminescence of and Schottky diodes from gold and)

L45 ANSWER 12 OF 13 HCA COPYRIGHT 2001 ACS

ACCESSION NUMBER: 115:196171 HCA
TITLE: Formation of multiple levels of **porous silicon** for buried insulators and conductors in silicon device technologies
INVENTOR(S): Blewer, Robert S.; Gullinger, Terry R.; Kelly, Michael J.; Tsao, Sylvia S.
PATENT ASSIGNEE(S): United States Dept. of Energy, USA
SOURCE: U.S., 11 pp.
CODEN: USXXAM
DOCUMENT TYPE: Patent
LANGUAGE: English
FAMILY ACC. NUM. COUNT: 1
PATENT INFORMATION:

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5023200	A	19910611	US 1988-274892	19881122
US 274892	A0	19920101		

AB A method for forming a multiple-level **porous Si substrate** for a semiconductor integrated circuit includes anodizing nonporous Si layers of a multilayer **Si substrate** to form multiple levels of **porous Si**. At least 1 **porous Si** layer is then **oxidized** to form an insulating layer and .gtoreq.1 other layer of **porous Si** beneath the insulating **layer** is **metalized** to form a buried conductive layer. Preferably, the insulating layer and conductive layer are sepd. by an anodization barrier formed of nonporous Si. By **etching** through the anodization barrier and subsequently forming a **metalized** conductive **layer**, a fully or partially insulated buried conductor may be fabricated under single-crystal Si.

IC ICM H01L021-44

NCL 437187000

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 72

ST multiple level **porous silicon** semiconductor device; buried insulator **porous silicon** semiconductor device; conductor buried **porous silicon** semiconductor device; anodization **porous silicon** semiconductor device

IT Electric conductors
Electric insulators and Dielectrics
(buried, multiple-level, formation of **porous silicon** for, for semiconductor devices)

IT Semiconductor devices
(formation of multiple-level **porous silicon** for buried insulators and conductors for)

IT **7664-39-3**, **Hydrogen fluoride**, uses and miscellaneous
(anodization by, for manuf. of semiconductor integrated circuits)

L45 ANSWER 13 OF 13 HCA COPYRIGHT 2001 ACS

ACCESSION NUMBER:	105:175859 HCA
TITLE:	Novel approach to efficient photoelectrochemical solar cells using electrolyte/discontinuous metal/semiconductor junctions
AUTHOR(S):	Nakato, Yoshihiro; Ueda, Keiichi; Tsubomura, Hiroshi
CORPORATE SOURCE:	Fac. Eng. Sci., Osaka Univ., Toyonaka, 560, Japan
SOURCE:	J. Phys. Chem. (1986), 90(22), 5495-6 CODEN: JPCHAX; ISSN: 0022-3654
DOCUMENT TYPE:	Journal
LANGUAGE:	English

AB The open-circuit voltage (Voc) of a photoelectrochem. cell with an n-Si electrode coated with a microscopically discontinuous **Pt layer** in an 8.8M HBr/0.05M Br aq. soln. is .apprx.0.05 V, whereas the Voc of a similar cell with an n-Si electrode coated with a continuous **Pt layer** was

.apprx..0.2 V. The discontinuous **Pt coatings** of
2.0 nm thickness were formed by deposition of Pt on photoetched n-Si
electrode by electron-beam evapn. The **Pt-coated**
n-**Si** electrodes, both **porous** and flat, were
stable in aq. redox solns. The Voc for the **porous**
Pt-coated Si electrode increases
linearly with the redox potential of I-I- couple, whereas the Voc
for Si with a continuous **Pt layer** is nearly
const., irresp. of the redox potential.

CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)

ST **platinum coating** silicon photoelectrochem cell;
photoetching silicon **platinum coating** electrodes

IT **Etching**
(photochem., of silicon, in **hydrofluoric acid**
, **platinum coating** and photoelectrochem.
application in relation to)

IT Electrodes
(photoelectrochem., **platinum coated** on
photoetched silicon, performance of, in redox electrolytes)

IT Photoelectric devices, solar
(photoelectrochem., **platinum-coated** silicon,
contg. aq. redox electrolytes, performance of)

IT Electric potential
(redox, of **silicon** coated with **porous** and
continuous **platinum layers**, in iodine-iodine
aq. soln.)

IT 7553-56-2, uses and miscellaneous 7726-95-6, uses and
miscellaneous
(electrolytes contg., in photoelectrochem. cells with
platinum-coated silicon electrodes)

IT **7664-39-3**, reactions
(photochem. **etching** by, of silicon, **platinum**
coating and photoelectrochem. application in relation to)

IT 7440-21-3, uses and miscellaneous
(**platinum-coated**, electrodes, for
photoelectrochem. cells)

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=> d his l51-

     FILE 'HCA' ENTERED

L51        18726 S ELECTROLESS? OR ELECTRO(2A)LESS?
L52           27 S L10 AND L51
L53            8 S L52 AND L11
L54            5 S L53 AND L16
L55            4 S L54 AND (L8 OR L15)
L56          563 S L37 AND L51
L57           51 S L56 AND L11 AND L16
L58           13 S L57 AND (L8 OR L15)
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L59             3 S L58 AND (L12 OR L13 OR L14 OR L30)
L60             6 S L58 AND (L26 OR L27 OR L28)
L61            12 S L58 AND L22
L62             4 S L57 AND L10
L63            11 S (L55 OR L59 OR L60 OR L61) NOT L45
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=> d l63 1-11 cbib abs hitind

L63 ANSWER 1 OF 11 HCA COPYRIGHT 2001 ACS

135:281051 New **porous silicon** formation technology using internal current generation with galvanic elements. Splinter, A.; Sturmann, J.; Benecke, W. (Institute for Microsensors, Microactuators, and Microsystems (IMSAS), University of Bremen, Bremen, D-28334, Germany). Sens. Actuators, A, A92(1-3, Light and Acoustics), 394-399 (English) 2001. CODEN: SAAPEB. ISSN: 0924-4247. Publisher: Elsevier Science S.A..

AB Presently, two **porous silicon** formation technologies are published, anodization in an electrochem. cell and stain **etch** without external current in a **hydrofluoric acid**/nitride **acid** (**HF**-HNO3) soln. For anodization an external current is necessary in order to achieve **porous silicon** thickness up to 100 .mu.m. Stain **etch** is an **electroless** process, and the porous layer thickness is limited to a few micrometers. A novel **porous silicon** formation technique that combines the advantages of thick layer anodization and **electroless** stain **etch** will be shown. A current generated by a galvanic element of silicon and a precious metal on the backside of a **silicon wafer** in a **hydrofluoric acid** (**HF**)/**hydrogen peroxide** (**H2O2**)/ethanol electrolyte is utilized in order to generate **porous silicon**. In this case the silicon operates as anode and the metal as cathode for current generation. This current is similar to the external current needed for anodization. Beside the std. **porous silicon etch** soln. **HF** and ethanol an **oxidizing** agent **H2O2** is used to support the **etch** process and to generate a higher **etch** rate. **Etch** rate control is given by concn. of **etching** soln. and metalization. Different kinds of metalizations and **etching** solns. were investigated.

CC 76-2 (Electric Phenomena)

ST **porous silicon** formation internal current galvanic element

IT Anodes
Cathodes
Electric current
Electrolytes
(new **porous silicon** formation technol. using internal current generation with galvanic elements)

IT Precious metals

(new **porous silicon** formation technol. using
internal current generation with galvanic elements)
IT 64-17-5, Ethanol, properties **7664-39-3**,
Hydrofluoric acid, properties **7722-84-1**,
Hydrogen peroxide, properties
(new **porous silicon** formation technol. using
internal current generation with galvanic elements)
IT **7440-21-3**, **Silicon**, properties
(**porous**; new **porous silicon**
formation technol. using internal current generation with
galvanic elements)

L63 ANSWER 2 OF 11 HCA COPYRIGHT 2001 ACS
130:244953 A study of immersion processes of activating polished crystalline silicon for autocatalytic **electroless** deposition of palladium and other metals. Karmalkar, S.; Banerjee, J. (Department of Electrical Engineering, Indian Institute of Technology (Madras), Chennai, 600 036, India). J. Electrochem. Soc., 146(2), 580-584 (English) 1999. CODEN: JESOAN. ISSN: 0013-4651. Publisher: Electrochemical Society.
AB The soln. in which Si is immersed for activation prior to autocatalytic **electroless** deposition (AED) of Ni, Cu, etc. is usually **HF**-PdCl2-HCl. However, we find that the AED of Pd on polished cryst. Si, which has important applications in modern planar integrated circuit technol., is non-adherent using this activator soln. The study of the effects of modifying this soln. and varying the substrate doping on the Pd deposition during activation and Pd AED adhesion reveals the following. The activation quality and hence AED adhesion depends not on the SiO2 **etch** rate of the soln. but on the compn. of the soln. Pd complex and the substrate hole concn. In spite of the highest Pd deposition rate during immersion, the activation quality of n-Si with doping >1019/cm3 is poor unless a hole-generating stimulus (e.g., illumination) is present. A change in substrate hole concn. influences AED adhesion by altering the substrate potential and/or d. of nucleation sites during activation. Similarly, a change in the Pd complex affects AED adhesion by altering the soln. Pd potential. Introduction of certain NH4+ compds. into the **HF** -PdCl2-HCl bath creates a specific Pd-ammine complex, most probably Pd(NH3)2 Cl2, which gives Pd AED adhesions of .apprx.9 and 4(3) .times. 106 N/m2 on heavily doped p-Si and lightly doped p(n)-Si, resp., using a low SiO2 **etch** rate (.apprx.90 .ANG./min) and a low temp. (200.degree.) for Pd nuclei silicidation during activation. The results regarding the activation mechanism are believed to apply generally to all AED on Si.
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 56
ST immersion activating polished cryst silicon autocatalytic **electroless** deposition palladium; nickel copper autocatalytic **electroless** deposition **silicon surface**; doping silicon boron phosphorus **oxidn** surface **etching**; complex palladium formation adhesion

metal **silicon surface**; ammonium hydroxide addn
activator system adhesion metal **silicon surface**
IT **Electroless** plating
Polishing
Wetting
(immersion processes of activating polished cryst. silicon for autocatalytic **electroless** deposition of palladium and other metals)
IT Integrated circuits
(immersion processes of activating polished cryst. silicon for autocatalytic **electroless** deposition of palladium and other metals for use in)
IT **Etching**
(of SiO2-surfaces for autocatalytic **electroless** deposition of palladium and other metals)
IT **Oxidation**
(of **silicon wafers** for autocatalytic **electroless** deposition of palladium and other metals)
IT Doping
(with boron and phosphorus of **silicon wafers** before autocatalytic **electroless** deposition of palladium and other metals)
IT 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
(as dopant for silicon in autocatalytic **electroless** deposition of palladium and other metals on **silicon surfaces**)
IT 14323-43-4, Diammine dichloro palladium 14349-67-8, Tetrachloro palladate (-2) 15974-14-8, Tetraammine palladium(2+)
(complex formed in autocatalytic **electroless** deposition of palladium and other metals on **silicon surfaces**)
IT 7647-01-0, Hydrogen chloride, processes 7647-10-1, Palladium chloride (PdCl2) **7664-39-3**, **Hydrogen fluoride**, processes
(component of soln. for activating polished cryst. silicon for autocatalytic **electroless** deposition of palladium and other metals)
IT 7440-02-0, Nickel, processes 7440-50-8, Copper, processes
(immersion processes of activating polished cryst. silicon for autocatalytic **electroless** deposition of)
IT **7440-05-3**, Palladium, processes
(immersion processes of activating polished cryst. silicon for autocatalytic **electroless** deposition of palladium and other metals)
IT **7440-21-3**, Silicon, properties
(p- and n- wafers; immersion processes of activating polished cryst. silicon for autocatalytic **electroless** deposition of palladium and other metals)
IT 67-64-1, Acetone, processes 79-01-6, Trichloroethylene, processes
(used for degreasing **surfaces** of **silicon wafers** for autocatalytic **electroless** deposition of palladium and other metals)

IT 7697-37-2, Nitric acid, processes
(used for removing metal impurities from **surfaces** of **silicon wafers** for autocatalytic **electroless** deposition of palladium and other metals)
IT 1336-21-6, Ammonium hydroxide 10039-56-2, Sodium hypophosphite monohydrate 12125-02-9, Ammonium chloride, processes
(used in a bath for autocatalytic **electroless** deposition of palladium and other metals)
IT 12125-01-8, Ammonium fluoride
(used in autocatalytic **electroless** deposition of palladium and other metals)

L63 ANSWER 3 OF 11 HCA COPYRIGHT 2001 ACS
126:323775 Atomic force microscopy study of the silicon doping influence on the first stages of platinum **electroless** deposition.
Gorostiza, Pau; Diaz, Raul; Servat, Jordi; Sanz, Fausto (Departament de Quimica Fisica, Universitat de Barcelona, Barcelona, E-08028, Spain). J. Electrochem. Soc., 144(3), 909-914 (English) 1997. CODEN: JESOAN. ISSN: 0013-4651. Publisher: Electrochemical Society.
AB The first stages of platinum **electroless** deposition on (100) Si from **hydrogen fluoride** solns. are studied by tapping-mode at. force microscopy (AFM), TEM microscopy, and XPS. Tapping-mode AFM and TEM provide a morphol. characterization of the samples, while XPS accounts for the compds. present on the surface. During immersion in an aq. **HF** soln. contg. a platinum salt, platinum nucleates on the **silicon substrate** while the surface is **etched**. The deposited nuclei are polycryst., highly pure, and strongly silicided at room temp. Metal deposition takes place by means of a redox reaction in which silicon atoms **oxidize**, supplying the electrons for the metal to reduce. For all substrates, platinum silicide is formed during deposition at room temp., suggesting a competition between the deposition of pure metal by an electrochem. mechanism and the formation of the silicide by direct reaction. For equal deposition times, more platinum deposits on p-type substrates than in n+. P-type substrates, moreover, undergo a general increase in roughness in the bare silicon areas, while n-type substrates present a lower and more local **etching**. This seems to indicate that **electroless** platinum deposition is somehow hindered on n+-substrates.
CC 76-2 (Electric Phenomena)
Section cross-reference(s): 56, 72
ST **silicon substrate electroless** deposition platinum; **hydrogen fluoride** soln **electroless** deposition platinum; atomic force microscopy **electroless** platinum deposition
IT Atomic force microscopy
Electroless plating
(at. force microscopic study of silicon doping effect on first stages of platinum **electroless** deposition)
IT **7440-21-3**, Silicon, uses

(**electroless** deposition of platinum on (100) Si from **hydrogen fluoride** soln.)
IT **7440-06-4**, Platinum, processes
(**electroless** deposition; at. force microscopic study of silicon doping effect on first stages of platinum **electroless** deposition)
IT **7664-39-3**, **Hydrogen fluoride**, uses
(soln.; at. force microscopic study of silicon doping effect on first stages of platinum **electroless** deposition)

L63 ANSWER 4 OF 11 HCA COPYRIGHT 2001 ACS
126:205974 Differences between N and P-type substrates in the platinum deposition on silicon. Gorostiza, Pau; Diaz, Rauel; Sanz, Fausto; Morante, Joan Ramon (Dep. Quimica Fisica, Univ. Barcelona, Barcelona, E-08028, Spain). Proc. - Electrochem. Soc., 96-19(Electrochemically Deposited Thin Films), 125-135 (English) 1997. CODEN: PESODO. ISSN: 0161-6374. Publisher: Electrochemical Society.
AB Platinum **electroless** deposition on silicon from **HF** solns. is studied by SEM and TEM, focusing on the different behavior of n and p-type samples. In both cases the **silicon substrate** is **etched** while platinum nucleates on the surface, and a complete **platinum layer** is eventually formed. The process seems to be hindered on n substrates and displays a more local behavior compared to p substrates. The results are discussed in terms of a global electrochem. redox reaction in which silicon is **oxidized** and platinum reduces injecting holes to the silicon valence band.
CC 76-3 (Electric Phenomena)
ST nitrogen **substrate** platinum deposition **silicon oxidn**
IT Crystal nucleation
Electrochemical redox reaction
Electroless plating
Etching
Oxidation
Valence band
(differences between N and P-type substrates in platinum deposition on silicon)
IT **7440-06-4**, Platinum, properties **7440-21-3**, Silicon, properties
(differences between N and P-type substrates in platinum deposition on silicon)

L63 ANSWER 5 OF 11 HCA COPYRIGHT 2001 ACS
125:156012 Method for manufacturing a cubically integrated circuit arrangement. Hoenlein, Wolfgang; Schwarzl, Siegfried (Siemens A.-G., Germany). U.S. US 5529950 A 19960625, 8 pp. (English). CODEN: USXXAM. APPLICATION: US 1995-377049 19950123. PRIORITY: DE 1994-4403736 19940207.
AB A method used in manufg. a cubically integrated circuit arrangement is described in which the resulting thinned substrates can be tested

from both sides. A **Si wafer**, wherein through
pores are produced by electrochem. **etching** are insulated
from the **Si wafer**, and are provided with
conductive fills, is secured as a carrier plate to a substrate that
has components and that is integrated in a cubically integrated
circuit arrangement. Terminal pads that are elec. connected to
conductive fills and that are arranged on the surface of the carrier
plate thereby meet contacts to the components that are arranged at
the surface of the substrate adjoining the carrier plate and that
are firmly connected thereto.

IC ICM H01L021-288
ICS H01L021-60

NCL 437170000

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 72

ST silicon electrochem **etching** cubic integrated circuit;
porous silicon cubic integrated circuit

IT **Etching**
(electrochem., manuf. of cubically integrated circuit with
substrate testable from both sides)

IT Coating process
(**electroless**, manuf. of cubically integrated circuit
with substrate testable from both sides)

IT Sputtering
(**etching**, manuf. of cubically integrated circuit with
substrate testable from both sides)

IT **Etching**
(sputter, manuf. of cubically integrated circuit with substrate
testable from both sides)

IT **Oxidation**
(thermal, manuf. of cubically integrated circuit with substrate
testable from both sides)

IT **7664-39-3**, **Hydrogen fluoride**, uses
(electrochem. **etchant**; manuf. of cubically integrated
circuit with substrate testable from both sides)

IT **7440-21-3**, Silicon, processes
(manuf. of cubically integrated circuit with substrate testable
from both sides)

L63 ANSWER 6 OF 11 HCA COPYRIGHT 2001 ACS

123:211186 Electrochemical coupling effects on the corrosion of silicon
samples in **HF** solutions. Torcheux, L.; Mayeux, A.;
Chemla, M. (Lab. d'analyse, IBM, Corbeil Essonnes, 91105, Fr.). J.
Electrochem. Soc., 142(6), 2037-46 (English) 1995. CODEN: JESOAN.
ISSN: 0013-4651.

AB Multilevel metalization commonly used in semiconductor manufg. for
VLSI and ULSI circuits prodn. requires low defect densities. In
particular, the authors could observe in some circumstances, a new
defect generation owing to a pitting corrosion of the polysilicon
substrate during wet processing. Polysilicon pitting corrosion was
studied in hydrofluoric solns. (DHF and BHF). The mechanism of
corrosion can proceed by two different modes. First, a purely

electroless mechanism can appear on a nearly homogeneous **surface** of **Si** where a few sites play the role of microcathodes; in that case, surface metallic contamination by metal impurities from hydrofluoric solns. is a source of Si corrosion. A study to characterize all intervening parameters is made using total reflectance x-ray fluorescence (TXRF). Second, a spontaneous difference of potential between Pt-Si plots and polysilicon electrode enhances the short-circuit current. A procedure is developed to study this corrosion in relation to real conditions existing during the wet process. This corrosion is analogous to the anodic dissoln. very near the thermodn. equil. value; then, a very small defect on the structure results in a local variation of potential, favorable to pitting or intergranular corrosion. Such a mechanism, at a low value of the overpotential and low c.d., is known to be responsible for a preferential **etching** on crystal lattice defects and leads to surface roughening and pinhole formation.

CC 72-2 (Electrochemistry)
Section cross-reference(s): 76

ST electrochem coupling effect corrosion silicon; **oxidn** electrochem silicon **hydrofluoric acid** soln; ammonium fluoride silicon corrosion

IT Impurities and Impurity centers
(electrochem. coupling effects on corrosion of silicon samples in **HF** solns. affected by metal impurities)

IT **Oxidation**
Oxidation, electrochemical
(electrochem. coupling effects on **oxidn**. of silicon samples in **HF** solns.)

IT Surface structure
(roughness, electrochem. coupling effects on corrosion of silicon samples in **HF** solns. with ammonium fluoride affected by roughness)

IT **7664-39-3**, **Hydrofluoric acid**, uses
12125-01-8, Ammonium fluoride
(electrochem. coupling effects on corrosion of silicon samples in **HF** solns.)

IT **7440-21-3**, Silicon, properties
(electrochem. coupling effects on corrosion of silicon samples in **HF** solns.)

IT 7439-89-6, Iron, occurrence 7440-02-0, Nickel, occurrence **7440-06-4**, Platinum, occurrence 7440-22-4, Silver, occurrence 7440-47-3, Chromium, occurrence 7440-50-8, Copper, occurrence 7440-66-6, Zinc, occurrence
(electrochem. coupling effects on corrosion of silicon samples in **HF** solns. affected by metal impurities)

L63 ANSWER 7 OF 11 HCA COPYRIGHT 2001 ACS

112:163173 **Electroless** plating of **silicon wafer** with nickel. Saito, Makoto; Shimada, Toshiaki; Akimoto, Koji; Ishikawa, Yutaka; Nakamichi, Ichiro (Nippon Inst. Tech., Saitamaken, Japan). Nippon Kogyo Daigaku Kenkyu Hokoku,

19(1), 31-4 (Japanese) 1989. CODEN: NKDHDG. ISSN: 0389-2514.
AB The **electroless** coating of **Si wafers** with Ni was studied. The process consisted of KOH treatment and **etching** in a soln. contg. **HF**, HNO3, CH3COOH, and **H2O2**. The Ni coating on n-type Si had satisfactory ohmic characteristic, independent of resistivity. For p-type Si with high resistivity, ohmic contact was obtained by annealing at 400.degree. for 5 min in N2 after **electroless** plating.
CC 56-6 (Nonferrous Metals and Alloys)
Section cross-reference(s): 76
ST nickel **electroless** coating **silicon wafer**
IT Coating process
(**electroless**, of **silicon wafers** with nickel)
IT **7440-21-3**, Silicon, uses and miscellaneous
(**electroless** coating of wafers of, with nickel)
IT 7440-02-0, Nickel, uses and miscellaneous
(**electroless** coating with, on **silicon wafers**)

L63 ANSWER 8 OF 11 HCA COPYRIGHT 2001 ACS
105:195646 The adhesion of **electroless** coating on **silicon wafer**. Shibuya, Tomoyoshi; Honma, Hideo (Fac. Eng., Kanto Gakuin Univ., Yokohama, 236, Japan). Kinzoku Hyomen Gijutsu, 37(9), 563-8 (Japanese) 1986. CODEN: KZHGAY. ISSN: 0026-0614.
AB The adhesion of **electroless** nickel coatings on a **Si wafer** was improved through **etching** of the wafer in a KOH soln. and in a **HF**-CH3COOH-**H2O2**-HNO3 soln. When the wafer was immersed in a hot KOH soln., it was **etched** with evolution of H, and the surface was hydrophilic. When it was immersed in a **HF**-HNO3-CH3COOH soln., many dimple-like pits were formed and the surface was hydrophilic. When it was immersed in a KOH soln. and in a **HF**-HNO3-CH3COOH soln. successively, the no. of pits increased, and the surface was still hydrophilic. When the wafer, treated in a KOH soln. and in acids, was again immersed in the mixt. of the acids after it was dried, many fine **etch** pits were formed, and the surface was hydrophobic. Addn. of **H2O2** to the mixt. of acids caused formation of **microetch** pits 0.5-1.5 .mu. in depth.
CC 56-6 (Nonferrous Metals and Alloys)
Section cross-reference(s): 76
ST silicon **etching** nickel **electroless** coating; potassium hydroxide **etching** silicon coating; acid **etching** silicon coating nickel; peroxide **etching** silicon coating nickel
IT **Etching**
(of **silicon wafer**, for nickel **electroless** coating)
IT Coating process
(**electroless**, of **silicon wafer**, with nickel, **etching** for)

IT **7440-21-3**, uses and miscellaneous
(**electroless** coating of wafer of, with nickel,
etching for)
IT 7440-02-0, uses and miscellaneous
(**electroless** coating with, of **silicon**
wafer, **etching** for)
IT **7722-84-1**, reactions
(**etching** by acid soln. contg., of **silicon**
wafer for nickel **electroless** coating)
IT 64-19-7, reactions 1310-58-3, reactions **7664-39-3**,
reactions 7697-37-2, reactions
(**etching** by soln. of, of **silicon**
wafer for nickel **electroless** coating)

L63 ANSWER 9 OF 11 HCA COPYRIGHT 2001 ACS
71:65415 Coating semiconductors with conducting **metal**
layers. Lepiane, Donald C. (Western Electric Co., Inc.).
Fr. FR 1535823 19680809, 5 pp. (French). CODEN: FRXXAK. PRIORITY:
US 19660920.
AB In prepg. semiconductors, crystals of Si, Ge, or III-V compds. are taken, and Group III or Group V elements are diffused into the crystal to form a p- or n-type semiconducting crystal. Thin wafers are then cut, and these are then doped from one side to produce p-n junctions. Each wafer is then cut into several hundred chips. A conductor must be attached to each surface of a chip, and it is difficult to obtain strong metal-substrate bonds with low elec. resistances. Elastic conductors, pressing against the surfaces, are easily disturbed by shocks or vibration, and soldering is not very successful, since it is difficult to wet the surface of the chip with solder. One of the most successful methods is **electroless** deposition of a conducting metal onto the surface of the wafer before it is cut into chips. However, any **oxidn**. of the wafer surface may produce, in the case of P-and B-doped Si, phosphosilicates on one surface, and borosilicates on the other. These compds. are removed in aq. **HF**, but at different rates, and if the immersion time is long enough to dissolve all the borosilicates, the P-doped surface is somehow rendered passive to **electroless** Ni deposition. Thus, each surface usually must be treated sep. to clean off the oxide layer. In the new method, a **Si wafer** is immersed in aq. **HF** to dissolve all the oxides, rinsed, and then immersed in warm aq. NH4OH. The P-doped surface is reactivated, and successful **electroless** Ni deposition is then carried out. Thus, after **etching** in aq. **HF** and rinsing, a P- and B-doped **Si wafer** was immersed 4-6 min. in aq. NH4OH at pH 8-10 at 80-90.degree., dried in air, immersed again in aq. **HF** for 3 min., rinsed, and immersed in the deposition soln.
IC C23C; H01L
CC 71 (Electric Phenomena)
ST semiconductors **metals coating**; **metals**
coating semiconductors; nickel coating semiconductors;
electro Ni coating semiconductors; silicon **electroless** Ni

coating; boron doped Si; phosphorus doped Si
IT Electric contacts
(nickel, to silicon contg. boron and phosphorus, surface pretreatment in **electroless** deposition of)
IT 7440-42-8, uses and miscellaneous 7723-14-0, uses and miscellaneous
(elec. contacts to **silicon** contg., **surface** pretreatment in **electroless** deposition of nickel)
IT **7440-21-3**, uses and miscellaneous
(elec. contacts to, contg. boron and phosphorus, surface pretreatment in **electroless** deposition of nickel)
IT 7440-02-0, uses and miscellaneous
(elec. contacts, surface pretreatment of boron- and phosphorus-contg. silicon in **electroless** deposition of)

L63 ANSWER 10 OF 11 HCA COPYRIGHT 2001 ACS
69:81647 Surface potential of anode-**oxidized** n-type **silicon surface**. Konorov, P. P.; Rushen, Yu.; Romanov, O. V.; Uritskii, V. Ya. (Leningrad. Gos. Univ. im. Zhdanova, Leningrad, USSR). Fiz. Tekh. Poluprov., 2(6), 840-2 (Russian) 1968. CODEN: FTPPA4.

AB n-Si single crystal slices cut along the (111) plane were polished, **etched** in HNO3 + **HF** soln., and provided with **electroless** Ni contacts. Anodic **oxidn**. was carried out in 0.04N KNO3 ethylene glycol solns. at a c.d. of 3 ma./cm.2 The thickness of the SiO2 layer was detd. with an interferential microscope or controlled by the resp. electrode potential. In ethylene glycol solns. freshly **etched** n-**Si surfaces** displayed a typical photo-potential of 200 mv. when illuminated with high intensity light. The variations of the electrode potential at different stages of anodic **oxidn**. reflected the resp. changes of the surface potential. Thus the 200-mv. photopotential corresponds to a basic carrier depleted surface layer. When a several A. thick SiO2 layer was formed, photopotential decreased to 10-20 mv. and remained const. up to 1500-1700 A. films, owing to alterations of the surface band structure. Exptl. cond.-potential curves of **etched** or anodically **oxidized** Si were plotted (in 0.1N Na2SO4 solns.) and juxtaposed with previous (C. Young, 1961) data based on theoretical surface cond. graphs. A discrepancy between the resp. figures is attributed to the substantial potential drop in the oxide layer during polarization in electrolytes and the decrease of cond. owing to the suppression of mobility by a surface scattering mechanism. Exptl. cond. data give +0.10 .+-. 0.02 v. as a typical value of surface potential in freshly **etched** Si, suggesting the presence of carrier depleted regions on the surface. When several A. thick SiO2 films are formed the resp. value increases to +0.15 v. Exptl. data provide evidence that the anodically **oxidized surface** of n-**Si** is substantially different from thermally **oxidized** enriched **Si surfaces**. The anodic SiO2 surface retains its properties in dry condition and shows no aging effects. It exhibits

a high d. of surface states as proved by the 30 v. potential region of nonlinear capacity changes. When such surfaces are annealed in N atm. at 320.degree. for 45 min. this region is reduced to 4 v. and the resp. d. of surface states decreases from 2 .times. 1012 to 1.2 .times. 1011/cm.2

CC 71 (Electric Phenomena)

ST **surface** potential **Si**; potential **surface** **Si**; **silicon** **surface** potential; **oxidized** Si potential

IT **Oxidation**
(of silicon (n-type), elec. surface potential in relation to anodic)

IT Electric potential
(**surface**, of **silicon** (n-type), anodic **oxidn**. effect on)

IT **7440-21-3**, properties
(elec. potential of surface of n-type, anodic **oxidn**. effect on)

L63 ANSWER 11 OF 11 HCA COPYRIGHT 2001 ACS

68:63756 Applying **metallic coatings**. Chuss, John T. (Western Electric Co., Inc.). Fr. FR 1486263 19670623, 5 pp. (French). CODEN: FRXXAK. PRIORITY: US 19650709.

AB A **metal coating** is applied to an area of a substrate surface after treating the substrate to impart a layer of oxide over the rest of the surface, depositing a porous film of a catalytic metal over the entire surface, treating the surface with a solvent capable of selectively dissolving only the oxide, and allowing just enough oxide to dissolve to remove the film of catalyst from the oxide layer. When metal is then deposited from an **electroless** plating soln., the coating forms only on the catalyst in the desired area. Thus, the **surface** of a **Si** (n-type) **wafer** is **oxidized**, masked, **etched** to expose an area of substrate, then doped with B (p-type). The oxides which form during the B diffusion are removed with a 2:1 mixt. of NH4F and **HF**. The wafer is dipped in an acid SnCl2 soln. to sensitize the surface, then in an acid PdCl2 soln. to activate the Sn film. Rinsing with deionized water follows each dip. Dip times are very short, .apprx.60 and 20-30 sec., resp., to insure the formation of a porous Sn-**Pd** catalyst **film** on the SiO2. A 2nd treatment with NH4F-**HF** floats the catalyst from the oxide layer in 5-7 sec. Finally, Ni is deposited over the catalyst film on the doped area of the wafer from a conventional NiCl2 **electroless** plating soln. Addnl. **coatings** of **metal** and (or) noble metals can be deposited by standard procedures. The product is a diode with a uniform, firmly adhering **metal coating** on the p-type Si.

IC H01L

CC 71 (Electric Phenomena)

ST **METAL COATINGS** APPLICATION; SILICON DIODES PRODN; DIODES PRODN

IT Electric contacts
(to silicon devices, deposition of nickel on **palladium** -tin **films** in manuf. of)
IT **7440-21-3P**, uses and miscellaneous
(devices, elec. contacts to, deposition of nickel in manuf. of)
IT 7440-02-0, uses and miscellaneous **7440-05-3**, uses and miscellaneous 7440-31-5, uses and miscellaneous
(in elec. contact manuf., to silicon devices)

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L46 ANSWER 1 OF 11 HCA COPYRIGHT 2001 ACS
135:156588 Determination of diffusion coefficient in quartz tubes for semiconductor manufg. heat treating equipment by metal analysis method. Marumo, Yoshinori; Suzuki, Kaname; Hayashi, Teruyuki; Tanahashi, Takashi (Tokyo Electron Ltd., Japan). PCT Int. Appl. WO 2001059189 A1 20010816, 72 pp. DESIGNATED STATES: W: JP, KR, US; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR. (English). CODEN: PIXXD2. APPLICATION: WO 2000-JP9381 20001228. PRIORITY: JP 2000-29807 20000207.
AB Manuf. of quartz tube and anal. of metal (such as copper) content in quartz tube for semiconductor manufg. equipment capable of heat treating a substrate without causing contamination, are described. A quartz specimen is immersed in **hydrofluoric acid** to expose a layer to be analyzed located at a prescribed depth. On the exposed surface, a chem.-**etching** liq. such as **hydrofluoric acid** or nitric acid is dripped to decomp. only an extremely thin layer to be analyzed. The decompn. liq. is quant. analyzed by use of at. absorption spectroscopy or similar anal. method to measure the metal concn. in the decompn. liq. From the difference in thickness before and after **etching** and the area of dripped **etching** liq., the vol. of the **etched** layer is obtained. From the vol. of **etched layer** and **metal** content in **etching** liq., the metal concn. throughout the quartz sample is detd. as well as the diffusion coeff. for the layers analyzed. With the obtained diffusion coeff. as index, quartz material in which metal diffuses with difficulty is sorted out and a quartz tube for semiconductor manufg. equipment can be fabricated.
IC ICM C30B035-00
ICS C03B020-00; C30B031-10
CC 57-1 (Ceramics)
Section cross-reference(s): 47, 79
IT **Etching**
(detn. of diffusion coeff. in quartz tubes for semiconductor manufg. heat treating equipment by metal anal. method)
IT 7647-01-0, Hydrochloric acid, processes **7664-39-3**, **Hydrofluoric acid**, processes 7664-93-9, Sulfuric acid, processes 7697-37-2, Nitric acid, processes **7722-84-1**, **Hydrogen peroxide** (

H2O2), processes
(**etching** soln.; detn. of diffusion coeff. in quartz tubes for semiconductor manufg. heat treating equipment by metal anal. method)
IT **7440-21-3P**, **Silicon**, preparation
(**wafer**, heat treatment; detn. of diffusion coeff. in quartz tubes for semiconductor manufg. heat treating equipment by metal anal. method)

L46 ANSWER 2 OF 11 HCA COPYRIGHT 2001 ACS
134:201603 **HF**-FET and its production. Cappelllani, Annalisa; Lustig, Bernhard; Elbel, Norbert; Schumann, Dirk (Infineon Technologies A.-G., Germany). PCT Int. Appl. WO 2001017008 A1 20010308, 27 pp. DESIGNATED STATES: W: JP, KR, US; RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (German). CODEN: PIXXD2. APPLICATION: WO 2000-EP8350 20000825. PRIORITY: DE 1999-19940758 19990827.
AB The invention relates to a method for producing an **HF**-FET. Doped source and drain regions are created in a substrate. A gate-insulation layer is applied via a channel region. A spacer structure is created above the substrate which separates the channel region from the source and drain regions. A continuous **metal layer** is deposited using this structure and the thickness of the **metal layer** is reduced to such an extent that elec. sep. self-aligned metal structures are formed above the source, drain and channel regions.
IC ICM H01L021-336
ICS H01L029-417; H01L021-28; H01L029-49; H01L029-423
CC 76-3 (Electric Phenomena)
IT Sputtering
(**etching**, reactive; high-frequency-FET and prodn.)
IT **Etching**
(sputter, reactive; high-frequency-FET and prodn.)
IT **Oxidation**
(thermal; high-frequency-FET and prodn.)
IT **7722-84-1**, **Hydrogen peroxide**, uses
(chem. mech. polishing; high-frequency-FET and prodn.)
IT **7440-21-3**, **Silicon**, processes
(**substrate**; high-frequency-FET and prodn.)

L46 ANSWER 3 OF 11 HCA COPYRIGHT 2001 ACS
133:171067 Aluminum spiking inspection method for semiconductor contacts. Lee, Ching-Ying (Vanguard International Semiconductor Corporation, Taiwan). U.S. US 6107201 A 20000822, 9 pp. (English). CODEN: USXXAM. APPLICATION: US 1995-430467 19950428.
AB A method for inspection which involves the complete and sequential removal of an Al contg. metalization **layer**, and other **metal** and insulator **layers**, from the **surface** of a **Si substrate**. The layers are removed through sequential chem. **etch** processes tailored specifically to the compn. of the individual layers. Upon removal of all layers, the **surface** of the **Si**

substrate is **etched** in a buffered aq.
etchant soln. The **surface** of the **Si**
substrate may then be inspected with the aid of an optical
microscope to det. level to which the Al contg. metalization layer
has spiked into the **Si substrate**.
IC ICM H01L021-66
ICS H01L021-44; H01L021-461
NCL 438688000
CC 76-3 (Electric Phenomena)
ST **etching** microscopy aluminum contact spiking
IT Electric contacts
Etching
Microscopy
Quality control
(aluminum spiking inspection method for semiconductor contacts)
IT **7440-21-3**, Silicon, processes
(aluminum spiking inspection method for semiconductor contacts)
IT 64-19-7, Acetic acid, uses 1336-21-6, Ammonium hydroxide
7664-39-3, **Hydrogen fluoride**, uses
7697-37-2, Nitric acid, uses **7722-84-1**, **Hydrogen**
peroxide, uses
(**etchant**; aluminum spiking inspection method for
semiconductor contacts)

L46 ANSWER 4 OF 11 HCA COPYRIGHT 2001 ACS
132:201936 Low-haze wafer treatment process and apparatus. Carlson,
Brent D.; Olson, Erik D.; Oikari, James R. (FSI International, Inc.,
USA). U.S. US 6037271 A 20000314, 7 pp. (English). CODEN:
USXXAM. APPLICATION: US 1998-176588 19981021.
AB A process is described for removing a plurality of layers of
different materials from a **substrate** having a **Si**
material **base**, .gtoreq.1 of the layers being a Si oxide
material and .gtoreq.1 other of the **layers** comprising a
metal layer located above the Si oxide layer. The
process includes treating the substrate with chem. formulations
adapted to successively remove the materials of the plurality of
layers until the **Si** material **base** is exposed,
the Si oxide layer being removed by treatment with **HF**, in
which the **HF** treatment to remove the Si oxide layer
comprises exposing the substrate to: initially, a dil. **HF**
soln. of .ltoreq.1.0% concn.; subsequently, a concd. **HF**
soln. of .apprx.2.5-10% concn.; and finally, a dil. **HF**
soln. of .ltoreq.1.0% concn.
IC ICM H01L021-00
NCL 438751000
CC 76-3 (Electric Phenomena)
IT **Etching**
(in low-haze wafer treatment)
IT 1336-21-6, Ammonium hydroxide ((NH4)(OH)) 7647-01-0, Hydrogen
chloride, processes **7664-39-3**, **Hydrogen**
fluoride, processes 7664-93-9, Sulfuric acid, processes
7722-84-1, **Hydrogen peroxide**, processes

(**etching** by; in low-haze wafer treatment)
IT **7440-21-3**, Silicon, processes
(low-haze wafer treatment process and app.)

L46 ANSWER 5 OF 11 HCA COPYRIGHT 2001 ACS
127:27220 Manufacture of thin-film semiconductor devices. Yamazaki, Shunpei (Semiconductor Energy Laboratory Co., Ltd. (SEL), Japan). Jpn. Kokai Tokkyo Koho JP 09107100 A2 19970422 Heisei, 13 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1995-233305 19950818. PRIORITY: JP 1995-219559 19950804.
AB The title process comprises crystn. of an amorphous Si film by annealing using a crystn.-enhancing metal catalyst in contact with the Si film, selective removal of silicide of the metal catalyst, and addnl. filling of region(s), where the silicide is removed, by melting of the **surface** of the **Si** film crystd.
The metal may be Ni, and Ni silicide(s) may be selectively removed by a **HF-H2O2** soln. Effects of silicides are
removed from the Si film.
IC ICM H01L029-786
ICS H01L021-336; H01L021-324; H01L027-12
CC 76-3 (Electric Phenomena)
IT Thin film transistors
(crystn. of silicon amorphous **films** with catalytic **metals** and removal of silicide of catalytic metals in prepn. of devices)
IT Semiconductor devices
(thin-film; crystn. of silicon amorphous **films** with catalytic **metals** and removal of silicide of catalytic metals in prepn. of devices)
IT **7722-84-1**, **Hydrogen peroxide**, reactions
(-**hydrofluoric acid** mixt.; for removal of
nickel silicides formed in catalytic crystn. of silicon amorphous films in prepn. of semiconductor devices)
IT **7664-39-3**, **Hydrofluoric acid**, reactions
(**etchant**, -**hydrogen peroxide** mixt.;
for removal of nickel silicides formed in catalytic crystn. of silicon amorphous films in prepn. of semiconductor devices)
IT **7440-21-3**, Silicon, processes
(film; crystn. of amorphous **films** with catalytic **metals** in manuf. of thin-film semiconductor devices)

L46 ANSWER 6 OF 11 HCA COPYRIGHT 2001 ACS
124:328270 Microcontact printing of alkanethiols on silver and its application in microfabrication. Xia, Younan; Kim, Enoch; Whitesides, George M. (Dep. Chem., Harvard Univ., Cambridge, MA, 02138, USA). J. Electrochem. Soc., 143(3), 1070-9 (English) 1996. CODEN: JESOAN. ISSN: 0013-4651.
AB This paper describes the use of microcontact printing (.mu.CP) to generate patterned self-assembled monolayers (SAMs) of alkanethiolates on the surfaces of evapd. films of silver. Using patterned SAMs of alkanethiolates as nanometer-thick resists, patterned microfeatures of silver with sizes down to .apprx.200 nm

were fabricated on Si/SiO2 by selective **etching** in aq. solns. contg. K2S2O3, K3Fe(CN)6, and K4Fe(CN)6. Complete **etching** of silver can be achieved more rapidly than that of gold: .apprx.20 s vs. .apprx.20 min for 50 nm thick **metal films** when similar ferricyanide **etchants** were used. Microstructures of silver produced by the present method have higher edge resoln. (typically, .apprx.20 nm vs. .apprx.100 nm) and far fewer defects (.apprx.10 pits/mm2 vs. .apprx.103 pits/mm2) than those of gold fabricated by a similar procedure. Silver lines (0.2 .mu.m in thickness, .apprx.50 .mu.m in width, and .apprx.5 mm in length) had the expected metallic cond. (.apprxeq.5.56 .times. 105 S/cm); parallel lines of silver (0.2.mu.m in thickness, .apprx.10 .mu.m in width, .apprx.1 mm in length, and sepd. by .apprx.10 .mu.m) were elec. isolated from each other. Aq. solns. contg. other coordinating ligands and **oxidants**, Fe(NO3)3, NH4OH/O2, NH4OH/**H2O2**, and H2NCH2COOH/**H2O2**, were also selective **etchants** for use with patterned SAMs of alkanethiolates on silver. Patterned structures of silver (50 nm thick) on Si/SiO2 could be used as secondary masks for **etching** of SiO2 in aq. solns. of **HF**/NH4F, and of Si(100) in aq. solns. of KOH and iso-propanol. Patterned films of silver (0.2 .mu.m thick) on **silicon wafers** could be used as masters to cast elastomeric stamps with surface relief to be used for .mu.CP. By choosing appropriate **etching** conditions, microparticles of MX (M = Ag; X = Cl, Br, I, OH, and SCN) could be formed in situ on the underivatized regions of the SAM-patterned surface during **etching** of silver.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): 76

ST microcontact printing alkanethiol monolayer silver; **etching** resist patterned alkanethiol monolayer silver

IT **Etching**
(microcontact printing of alkanethiols on silver and its application in microfabrication)

IT Resists
(patterned SAMs of alkanethiolates as nanometer-thick **etching** resists on silver)

IT 56-40-6, Glycine, processes 151-50-8, Potassium cyanide 333-20-0, Potassium thiocyanide 1336-21-6, Ammonium hydroxide 7447-40-7, Potassium chloride, processes 7553-56-2, Iodine, processes 7681-11-0, Potassium iodide, processes 7705-08-0, Iron trichloride, processes **7722-84-1**, **Hydrogen peroxide**, processes 7758-02-3, Potassium bromide, processes 10294-66-3, Potassium thiosulfate 10421-48-4, Iron trinitrate 13746-66-2, Potassium ferricyanide 13943-58-3, Potassium ferrocyanide
(**etchant**; microcontact printing of alkanethiols on silver and its application in microfabrication)

IT **7440-21-3**, Silicon, processes 7440-22-4, Silver, processes 7440-57-5, Gold, processes 7631-86-9, Silica, processes **7664-39-3**, **Hydrogen fluoride**, processes

7782-44-7, Oxygen, processes 12125-01-8, Ammonium fluoride
(microcontact printing of alkanethiols on silver and its application in microfabrication)

L46 ANSWER 7 OF 11 HCA COPYRIGHT 2001 ACS
123:243220 Preventing noble metal contamination during silicon processing. Obeng, Yaw S. (AT&T Bell Laboratories, Allentown, PA, 18103, USA). Semicond. Pure Water Chem. Conf., 13th, 110-34 (English) 1994. CODEN: SPWCFI.
AB Noble metals contamination of **Si wafers** during **etching** in **HF** and/or NH4OH-**H2O2** and their impact on device yields are described from electrochem. perspectives. The observations are discussed in terms of redox processes at the Si-soln. interface during **etching**, and at the Si/film interface during high temp. processing. A guide for identifying potential metallic contaminants, and contamination extents are proposed, and theor. limits to metallic ions in **etchants** compared with the 1993 com. ULSI grade specifications. Strategies for preventing metallic contamination are also discussed.
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 48
IT **Etching**
Passivation
Process control and dynamics
Redox reaction
(preventing noble metal contamination during silicon processing)
IT **Oxidation**
(surface, preventing noble metal contamination during silicon processing)
IT 7631-86-9, Silica, processes
(passivation **layer**; preventing noble **metal** contamination during silicon processing)
IT 1336-21-6, Ammonium hydroxide ((NH4)(OH)) **7664-39-3**, **Hydrogen fluoride**, processes
(preventing noble metal contamination during silicon processing)
IT **7440-21-3**, Silicon, processes
(preventing noble metal contamination during silicon processing)
IT **7722-84-1**, **Hydrogen peroxide**, reactions
(preventing noble metal contamination during silicon processing)

L46 ANSWER 8 OF 11 HCA COPYRIGHT 2001 ACS
121:146865 Peroxide clean before buried contact polysilicon deposition. Chien, Sun-Chieh; Liu, Yu-Ju (United Microelectronics Corp., Taiwan). U.S. US 5328867 A 19940712, 11 pp. (English). CODEN: USXXAM. APPLICATION: US 1993-57881 19930507.
AB A method of removing impurities from the surface of an integrated circuit and forming a uniform thin native oxide layer on the same surface of an integrated circuit is described. A **HF** soln., followed by a rinse and spin dry, is often used to remove gate oxide from within an opening **etching** in a polysilicon layer. The rinsing leaves water spots. Spin drying leaves

impurities where water tracks were. An **H2O2** cleaning is performed to remove the water spots. After the cleaning, a uniform thin layer of native oxide is formed on the **surface** of the **silicon substrate**. A 2nd layer of polysilicon is deposited over the 1st thin native oxide layer and doped with an implant dosage chosen so that it will go through the uniform native oxide layer. The substrate is annealed to drive in the buried contact. Processing continues to form polysilicon or silicide gate electrodes. Spacers are formed on the sidewalls of the gate electrodes. An insulating layer is deposited over the **surface** of the **Si substrate**. Contact openings are **etched** through the insulating layer and filling the openings to the 2nd polysilicon layer and the **silicon substrate**. The **metal layer** is patterned, completing the formation of the buried contacts within the integrated circuits.

IC ICM H01L021-44
NCL 437191000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 49
IT 1336-21-6, Ammonium hydroxide **7722-84-1**, **Hydrogen peroxide**, uses
(cleaning by, before buried contact polysilicon deposition)
IT **7664-39-3**, **Hydrogen fluoride**, reactions
(**etching** by, of polysilicon layers, with removal of spots left by rinsing)
IT **7440-21-3**, Silicon, properties
(polycryst., deposition of, peroxide cleaning before buried contact)

L46 ANSWER 9 OF 11 HCA COPYRIGHT 2001 ACS
116:238746 Peeled film gallium arsenide solar cell development. Wilt, D. M.; Thomas, R. D.; Bailey, S. G.; Brinker, D. J.; DeAngelo, F. L.; Fatemi, N. S.; Landis, G. A. (Lewis Res. Cent., NASA, Cleveland, OH, 44135, USA). Conf. Rec. IEEE Photovoltaic Spec. Conf., 21st(1), 111-14 (English) 1990. CODEN: CRCNDP. ISSN: 0160-8371.
AB Thin film, single crystal GaAs p and n layers were fabricated using the peeled **film** technique by **metalorg**. vapor phase epitaxy on a GaAs substrate with AlAs parting layer. A wax layer was air-brushed on the epitaxy layer and cured at 160.degree. to produce a suitable compressive force for the peeling process; a **H2O2**/NH4OH was used as **etchant** to remove the AlAs layer. The peeled GaAs film was placed on a clean **Si** or glass **substrate**, the wax was removed by vapor degreasing, and back contacts were deposited by electron beam evapn. A GaAs solar cell, although formed with a fractured film and without window and antireflective layers, attained an open circuit voltage of 874 mV and a fill factor of 68% under air mass 0 illumination.
CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
Section cross-reference(s): 76
IT **7664-39-3**, **Hydrogen fluoride**, uses
(**etchants** of aq., for selective removal of aluminum

arsenide, in gallium arsenide solar cell manuf.)
IT **7722-84-1**, **Hydrogen peroxide**, uses
(**etchants**, contg. ammonia, for removal of aluminum
arsenide, in gallium arsenide solar cell manuf.)
IT 1336-21-6, Ammonium hydroxide
(**etchants**, contg. **hydrogen peroxide**
, for removal of aluminum arsenide, in gallium arsenide solar
cell manuf.)
IT **7440-21-3**, **Silicon**, uses
(**substrates**, gallium arsenide peeled films on, solar
cell fabrication using)

L46 ANSWER 10 OF 11 HCA COPYRIGHT 2001 ACS
113:143502 Preparation of electric contacts in semiconductor-device
manufacture. Nishida, Soichi (Matsushita Electronics Corp., Japan).
Jpn. Kokai Tokkyo Koho JP 02112262 A2 19900424 Heisei, 4 pp.
(Japanese). CODEN: JKXXAF. APPLICATION: JP 1988-265761 19881021.
AB Manuf. of a semiconductor device includes: (a) forming a
gate-insulator film on a **Si substrate**; (b)
depositing polycryst. Si on the insulator film; (c) **etching**
-off part of the Si film with the use of a photoresist pattern; (d)
after removing the resist pattern, ion-implanting an n-type impurity
with a d. of .gtoreq.1 .times. 1015/cm2; (e) removing the
gate-insulator film inside the Si-film opening with a mixt. of an
aq. soln. of NH3 and **H2O2**; (f) annealing the substrate;
(g) removing a neutral oxide film with, e.g., **HF**, and (h)
forming a refractory-**metal**-silicide **film** on the
whole surface by chem. vapor deposition or sputter deposition. The
method does not contaminate the gate-insulator film.
IC ICM H01L021-90
ICS H01L021-28; H01L021-3205
CC 76-3 (Electric Phenomena)
IT **7440-21-3**, Silicon, uses and miscellaneous
(polycryst., in prepn. of elec. contacts for semiconductor
devices)

L46 ANSWER 11 OF 11 HCA COPYRIGHT 2001 ACS
93:196550 **Etchant** solution containing **hydrogen
fluoride**-nitric acid-sulfuric acid-**hydrogen
peroxide** for **etching** aluminum-titanium-copper or
nickel contact metallurgy or **silicon substrates**.
Spak, Mark A. (RCA Corp., USA). U.S. US 4220706 19800902, 3 pp.
(English). CODEN: USXXAM. APPLICATION: US 1978-904541 19780510.
AB An **etchant** is described for use at .apprx.25-65.degree. in
the manuf. of metalization for power devices, such as Si controlled
rectifiers, horizontal deflector transistors, etc., where several
metals are applied over glass or **Si**-contg.
surfaces. Three **metal layers** in
particular are considered: (1) Al (0.1-8 .mu.m), (2) Ti, Mo, or W
(0.2-0.7 .mu.m), and (3) Ni or Cu (0.4-2 .mu.m). An **etchant**
for these layers comprises HNO3 0.5-50, **HF** 0.03-1.0,
H2O2 0.05-0.5, and H2SO4 0.1-1.0 wt. % in aq. soln. It

etches the metals at a uniform rate, is compatible with conventional photoresists, does not promote interaction between the metals during **etching**, and has a min. effect on insulating substrates.
IC H01L021-44; H01L021-465; H01L021-88
NCL 430318000
CC 76-13 (Electric Phenomena)
ST **etching** triple layer metalization; semiconductor multilayer metalization **etching**
IT Semiconductor devices
(**etching** of triple-layer metalization structures for)
IT Electric conductors
(interconnection, **etching** of triple-layer, in semiconductor devices)
IT **Etching**
(of triple-layer metalization structures for semiconductor devices)
IT **7440-21-3**, uses and miscellaneous
(devices, **etching** of triple-layer metalization structures for)
IT 7429-90-5, reactions 7439-98-7, reactions 7440-02-0, reactions
7440-32-6, reactions 7440-33-7, reactions 7440-50-8, reactions
(**etching** of patterns in triple-layer metalization structures from, for semiconductor devices)

=> d 147 1-6 cbib abs hitind

L47 ANSWER 1 OF 6 HCA COPYRIGHT 2001 ACS
132:328632 Method of fabricating embedded gate electrodes. Chen, Chih-rong; Yeh, Chi-chin (United Microelectronics Corp., Taiwan). U.S. US 6066532 A 20000523, 12 pp. (English). CODEN: USXXAM. APPLICATION: US 1999-419434 19991018.
AB A method of fabricating an embedded gate electrode is disclosed. The method includes the steps of: Providing a semiconductor substrate; forming a patterned **etch** resistant mask layer over the semiconductor substrate, wherein the patterned **etch** resistant mask layer has a 1st opening for a desired location of a trench; anisotropically **etching** through the patterned **etch** resistant mask layer and into the semiconductor substrate, hence forming the trench at the desired location; removing the patterned **etch** resistant mask layer; depositing a 1st insulating layer over the semiconductor substrate and filling up the trench; patterning a planarized 1st insulating layer to define a 2nd opening for the embedded gate electrode; forming a 2nd insulating layer at the bottom of the 2nd opening; depositing a conductive layer over the 2nd insulating layer and filling up the 2nd opening, hence forming the embedded gate electrode; ion implanting the semiconductor substrate to form source/drain regions; forming a spacer on the sidewall of the embedded gate electrode; depositing a refractory **metal**

layer over the entire exposing surface of a resulting structure; and annealing the refractory **metal** **layer** to form a silicide layer on the embedded gate electrode and elsewhere on the source/drain regions.

IC ICM H01L021-336

NCL 438259000

CC 76-3 (Electric Phenomena)

IT **Etching**
(anisotropic; in method of fabricating embedded gate electrodes)

IT Annealing
Cleaning
Dielectric films
Electron beam evaporation
Etching masks
Ion implantation
Magnetron sputtering
Photolithography
Rapid thermal annealing
Siliconizing
(in method of fabricating embedded gate electrodes)

IT **Etching**
(selective; in method of fabricating embedded gate electrodes)

IT 7664-38-2, Phosphoric acid, uses
(**etchant** for silicon nitride; in method of fabricating embedded gate electrodes)

IT **7440-21-3**, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
(in method of fabricating embedded gate electrodes)

IT 67-63-0, Isopropanol, uses 1310-58-3, Potassium hydroxide, uses **7664-39-3**, **Hydrogen fluoride**, uses 7664-93-9, Sulfuric acid, uses **7722-84-1**, **Hydrogen peroxide**, uses
(in method of fabricating embedded gate electrodes)

L47 ANSWER 2 OF 6 HCA COPYRIGHT 2001 ACS

132:145419 Silicon nitride-TEOS oxide layer for blocking the formation of salicide in deep sub-micron devices. Pey, Kin-Leong; Siah, Soh-Yun; Lee, Yong-Meng (Chartered Semiconductor Manufacturing, Ltd., Singapore). U.S. US 6025267 A 20000215, 10 pp. (English). CODEN: USXXAM. APPLICATION: US 1998-115724 19980715.

AB A method for forming self-aligned **metal** silicide (salicide) **layers** on polysilicon gate structures and on source/drain regions located in a 1st region of a semiconductor substrate, while avoiding salicide formation on polysilicon gate structures and on source/drain regions located in a 2nd region of the substrate is described. A composite insulator shape, comprising an overlying Si nitride layer and an underlying TEOS deposited Si oxide layer, is used to block polysilicon as well as Si regions in the 2nd region of the semiconductor substrate from salicide formation. Unwanted Si oxide spacers, created on the sides of polysilicon gate structures during the patterning of the composite insulator shape, are selectively removed using dil. **HF**

solns.
IC ICM H01L021-46
NCL 438656000
CC 76-3 (Electric Phenomena)
IT **Etching**
(sputter, ion-beam, reactive; in manuf. of deep sub-micron devices using silicon nitride-TEOS oxide layer for blocking formation of salicide)
IT 1336-21-6, Ammonium hydroxide ((NH4)(OH)) 7647-01-0, Hydrogen chloride, processes **7722-84-1**, **Hydrogen peroxide**, processes
(**etching** by; in manuf. of deep sub-micron devices using silicon nitride-TEOS oxide layer for blocking formation of salicide)
IT 2551-62-4, Sulfur fluoride (SF6) **7664-39-3**, **Hydrogen fluoride**, processes 7782-44-7, Oxygen, processes 10035-10-6, Hydrogen bromide, processes
(**etching** by; in manuf. of deep sub-micron devices using silicon nitride-TEOS oxide layer for blocking formation of salicide)
IT **7440-21-3**, Silicon, processes
(silicon nitride-TEOS oxide layer for blocking formation of salicide in deep sub-micron devices contg.)

L47 ANSWER 3 OF 6 HCA COPYRIGHT 2001 ACS
129:103033 Method of forming a trench structure in a semiconductor device. Liang, Kuei-chang (Winbond Electronics Corp., Taiwan). U.S. US 5776817 A 19980707, 10 pp. (English). CODEN: USXXAM. APPLICATION: US 1997-779155 19970103. PRIORITY: TW 1996-85112174 19961004.
AB The invention relates to a method of forming trenches having different depths in a substrate of an IC using different refractory **metal layers**. The depths of the trenches can be changed by controlling the thicknesses of the refractory **metal layers**. The profiles of the trenches can also be changed by controlling operating parameters, such as temp. and reaction time.
IC ICM H01L021-76
NCL 438427000
CC 76-3 (Electric Phenomena)
IT **Etching**
(in formation of trench structures in semiconductor devices)
IT **7664-39-3**, **Hydrogen fluoride**, processes 7664-93-9, Sulfuric acid, processes **7722-84-1**, **Hydrogen peroxide**, processes
(**etching** by; in formation of trench structures in semiconductor devices)
IT **7440-21-3**, Silicon, processes
(formation of trench structures in semiconductor devices contg.)

L47 ANSWER 4 OF 6 HCA COPYRIGHT 2001 ACS
127:340502 Fabricating a MOSFET having local channel doping and a

titanium silicide gate. Tseng, Horng-huei (Vanguard International Semiconductor Corp., Taiwan). U.S. US 5677217 A 19971014, 10 pp. (English). CODEN: USXXAM. APPLICATION: US 1996-691287 19960801.

AB A process is described in which a deep submicron MOSFET is fabricated, featuring a local, narrow threshold voltage adjusting region in a semiconductor substrate, with the threshold voltage adjusting region self-aligned to an overlying, narrow, polycide gate structure. The process consists of forming a narrow hole in an insulator layer overlying a polysilicon layer and a gate insulator layer. Ion implantation through the polysilicon layer and gate insulator layer is used to place a narrow threshold voltage adjusting region in the specific area of the semiconductor substrate underlying the narrow hole. Deposition of a **metal layer**, followed by annealing, converts the top portion of the polysilicon in the narrow hole to a metal silicide. After removal of unreacted metal and the insulator layer, the polysilicon layer is patterned by RIE, using the metal silicide structure as a mask, to create a narrow polycide gate structure, comprised of an overlying, narrow metal silicide gate and an underlying, narrow polysilicon gate structure. The narrow polycide gate structure is self-aligned to the underlying, narrow threshold voltage adjusting region.

IC ICM H01L021-265

NCL 437045000

CC 76-3 (Electric Phenomena)

IT Annealing
Ion implantation
Reactive ion **etching**
(in fabricating a MOSFET having local channel doping and a titanium silicide gate)

IT 75-46-7, Fluoroform 2551-62-4, Sulfur fluoride (SF_6) **7664-39-3**, **Hydrogen fluoride**, processes 7664-93-9, Sulfuric acid, processes **7722-84-1**, **Hydrogen peroxide**, processes 10035-10-6, Hydrogen bromide, processes
(**etching** by; in fabricating a MOSFET having local channel doping and a titanium silicide gate)

IT **7440-21-3**, Silicon, processes
(polycryst.; fabricating a MOSFET having local channel doping and a titanium silicide gate contg.)

L47 ANSWER 5 OF 6 HCA COPYRIGHT 2001 ACS

125:183480 Manufacture of semiconductor device including capacitor. Tsunoda, Katsumi; Hirai, Masahiko (Asahi Chemical Ind, Japan). Jpn. Kokai Tokkyo Koho JP 08181102 A2 19960712 Heisei, 17 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1994-322445 19941226.

AB The device, with a capacitor comprising an under electrode, an insulating film, and an upper electrode formed on a substrate, is manufd. by leveling the surface of the under electrode on a field-oxide film by an isotropically chem.-dry **etching**, and chem.-washing it with no damage to the surface flatness. The under electrode may be Si, and the chem.-washing may use an aq.

soln. of NH3-**H2O2** or **HF**. The under electrode may be **metal** silicide **film** and the chem. washing may use an aq. soln. of NH3-**H2O2**, HCl-**H2O2**, or CH3CO2H-NH3. By the leveling and washing, electrodes in the capacitor have uniform effective-surface areas, showing improved voltage resistance and precision.

IC ICM H01L021-306
ICS H01L021-3065; H01L027-04; H01L021-822
CC 76-10 (Electric Phenomena)
ST semiconductor device capacitor electrode leveling; **etching** washing electrode surface semiconductor
IT **Etching**
(dry, leveling method for capacitor electrode of semiconductor device)
IT 64-19-7, Acetic acid, uses 7647-01-0, Hydrochloric acid, uses **7664-39-3**, **Hydrofluoric acid**, uses
7664-41-7, Ammonia, uses **7722-84-1**, **Hydrogen peroxide**, uses
(**etchant**; leveling method for capacitor electrode of semiconductor device)
IT 75-73-0, Tetrafluoromethane 7782-44-7, Oxygen, uses
(**etching** gas; leveling method for capacitor electrode of semiconductor device)
IT **7440-21-3**, Silicon, processes
(polycryst., under electrode; leveling method for capacitor electrode of semiconductor device)

L47 ANSWER 6 OF 6 HCA COPYRIGHT 2001 ACS
124:330014 Semiconductor device for thin-film transistor and its manufacture. Oonuma, Hideto; Adachi, Hiroki (Handotai Energy Kenkyusho, Japan). Jpn. Kokai Tokkyo Koho JP 08046209 A2 19960216 Heisei, 8 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1994-197363 19940729.
AB The device has an activating layer contg. a source region, a drain region, and a channel region, where .gtoreq.50-.ANG. surface layer of the source region and the drain region are **etched** and optionally the source region and the drain region are **coated** with a **metal** compd. **layer**. The device is manufd. by implanting an impurity ion into a source region and a drain region, **etching** the surface of the source region and the drain region, and optionally forming a **metal** compd. **layer** on the source region and the drain region. The device is manufd. by implanting an impurity ion into a source region and a drain region, removing the damaged surface of the source region and the drain region, and optionally forming a **metal** compd. **layer** on the source region and the drain region. Damage of the source region and the drain region in ion implantation was prevented.
IC ICM H01L029-786
ICS H01L021-336; H01L021-265
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75

IT Crystallization
Etching
(thin-film transistor and its manuf. for damage prevention in implantation of impurity ions)
IT 1336-21-6, Ammonium hydroxide **7664-39-3**, **Hydrofluoric acid**, uses 7697-37-2, Nitric acid, uses **7722-84-1**, **Hydrogen peroxide**, uses
(**etchant**; thin-film transistor and its manuf. for damage prevention in implantation of impurity ions)
IT 7429-90-5, Aluminum, processes **7440-21-3**, Silicon, processes 11116-16-8, Titanium nitride
(thin-film transistor and its manuf. for damage prevention in implantation of impurity ions)

=> d l48 1-15 cbib abs hitind

L48 ANSWER 1 OF 15 HCA COPYRIGHT 2001 ACS
135:281051 New **porous silicon** formation technology using internal current generation with galvanic elements. Splinter, A.; Sturmann, J.; Benecke, W. (Institute for Microsensors, Microactuators, and Microsystems (IMSAS), University of Bremen, Bremen, D-28334, Germany). Sens. Actuators, A, A92(1-3, Light and Acoustics), 394-399 (English) 2001. CODEN: SAAPEB. ISSN: 0924-4247. Publisher: Elsevier Science S.A..
AB Presently, two **porous silicon** formation technologies are published, anodization in an electrochem. cell and stain **etch** without external current in a **hydrofluoric acid**/nitride **acid** (**HF**-HNO3) soln. For anodization an external current is necessary in order to achieve **porous silicon** thickness up to 100 .mu.m. Stain **etch** is an electroless process, and the porous layer thickness is limited to a few micrometers. A novel **porous silicon** formation technique that combines the advantages of thick layer anodization and electroless stain **etch** will be shown. A current generated by a galvanic element of silicon and a precious metal on the backside of a **silicon wafer** in a **hydrofluoric acid** (**HF**)/**hydrogen peroxide** (**H2O2**)/ethanol electrolyte is utilized in order to generate **porous silicon**. In this case the silicon operates as anode and the metal as cathode for current generation. This current is similar to the external current needed for anodization. Beside the std. **porous silicon** **etch** soln. **HF** and ethanol an oxidizing agent **H2O2** is used to support the **etch** process and to generate a higher **etch** rate. **Etch** rate control is given by concn. of **etching** soln. and metalization. Different kinds of metalizations and **etching** solns. were investigated.

CC 76-2 (Electric Phenomena)
ST **porous silicon** formation internal current
galvanic element
IT Anodes
Cathodes
Electric current
Electrolytes
(new **porous silicon** formation technol. using
internal current generation with galvanic elements)
IT Precious metals
(new **porous silicon** formation technol. using
internal current generation with galvanic elements)
IT 64-17-5, Ethanol, properties **7664-39-3**,
Hydrofluoric acid, properties **7722-84-1**,
Hydrogen peroxide, properties
(new **porous silicon** formation technol. using
internal current generation with galvanic elements)
IT **7440-21-3**, **Silicon**, properties
(**porous**; new **porous silicon**
formation technol. using internal current generation with
galvanic elements)

L48 ANSWER 2 OF 15 HCA COPYRIGHT 2001 ACS
135:131476 Experimental Factors Controlling Analyte Ion Generation in Laser Desorption/Ionization Mass Spectrometry on **Porous Silicon**. Kruse, Rebecca A.; Li, Xiuling; Bohn, Paul W.; Sweedler, Jonathan V. (Department of Chemistry Beckman Institute for Advanced Science and Technology and Fredrick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL, 61801, USA). Anal. Chem., 73(15), 3639-3645 (English) 2001. CODEN: ANCHAM. ISSN: 0003-2700. Publisher: American Chemical Society.

AB Desorption/ionization on **porous silicon** (DIOS) is a relatively new laser desorption/ionization technique for the direct mass spectrometric anal. of a wide variety of samples without the requirement of a matrix. **Porous silicon substrates** were fabricated using the recently developed non-electrochem. **H2O2**-metal-**HF etching** as a versatile platform for studying the effects of morphol. and phys. properties of **porous silicon** on DIOS-MS performance. In addn., laser wavelength, mode of ion detection, pH, and solvent contributions to the desorption/ionization process were studied. Other porous substrates such as GaAs and GaN, with similar surface characteristics but differing in thermal and optical properties from **porous silicon**, allowed the roles of surface area, optical absorption, and thermal conductivities in the desorption/ionization process to be studied. Among the porous semiconductors studied, only **porous silicon** has the combination of large surface area, optical absorption, and thermal cond. required for efficient analyte ion generation under the conditions studied. In addn. to these substrate-related factors, surface wetting, detd. by the interaction

of deposition solvent with the surface, and charge state of the peptide are important in detg. ion generation efficiency.

CC 80-6 (Organic Analytical Chemistry)
Section cross-reference(s): 34

ST analyte ion generation laser desorption ionization mass spectrometry; ion generation laser desorption ionization mass spectrometry **porous silicon**

IT Peptides, analysis
(peptide detn. by laser desorption/ionization mass spectrometry on **porous silicon**)

IT Laser ionization mass spectrometry
(photodesorption; exptl. factors controlling analyte ion generation in laser desorption/ionization mass spectrometry on **porous silicon**)

IT Laser desorption mass spectrometry
(photoionization; exptl. factors controlling analyte ion generation in laser desorption/ionization mass spectrometry on **porous silicon**)

IT 686-50-0 9041-90-1, Angiotensin I 16875-11-9, Des-Arg1 bradykinin 17355-11-2 58822-25-6, Leu-enkephalin 77286-90-9 81733-79-1, (D-Ala2-Leu5-Arg6)-enkephalin 87549-53-9
(peptide detn. by laser desorption/ionization mass spectrometry on **porous silicon**)

IT 7440-21-3, Silicon, analysis
(peptide detn. by laser desorption/ionization mass spectrometry on **porous silicon**)

L48 ANSWER 3 OF 15 HCA COPYRIGHT 2001 ACS

134:215357 Wet **etching** of **porous silicon**.

Zhou, Wei; Fukuda, Yoshio; Furuya, Kazuo (Institute of Nuclear Energy Technology, Tsinghua University, Beijing, 100084, Peop. Rep. China). Dianzi Yuanjian Yu Cailiao, 19(5), 7-8 (Chinese) 2000. CODEN: DYCAFE. ISSN: 1001-2028. Publisher: Dianzi Yuanjian Yu Cailiao.

AB The **porous Si** layer prepd. by anodization was treated by wet **etching** with 1% **HF** soln., 1% NH3/**H2O2** soln., and 0.05% NaOH soln. The **porous Si** layer was studied by FTIR and SEM before and after wet **etching**. FTIR showed that the no. of Si-O and H-O bonds increased while that of Si-H bonds decreased after treatment with 1% NH3/**H2O2** soln., which were opposite to that of treatment with 0.05% NaOH and 1% **HF** solns. The **etching** rate of 0.05% NaOH soln. was higher than that of 1% **HF** soln., and the Si layer **etched** with NaOH soln. had the same anisotropic property as that of single cryst. **Si wafer etched** with strong alkali soln.

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 72, 73

ST **porous silicon** anodization wet **etching**

IT IR spectroscopy
(Fourier-transform; wet **etching** of **porous silicon**)

IT Bond
(hydrogen-silicon, by FTIR; wet **etching** of **porous silicon**)
IT Bond
(oxygen-silicon, by FTIR; wet **etching** of **porous silicon**)
IT Anodization
Etching
(wet **etching** of **porous silicon**)
IT **7440-21-3**, **Silicon**, properties
(**porous**; wet **etching** of **porous silicon**)
IT 1310-73-2, Sodium hydroxide, uses **7664-39-3**, **Hydrofluoric acid**, uses 7664-41-7, Ammonia, uses **7722-84-1**, **Hydrogen peroxide**, uses
(wet **etching** soln.; wet **etching** of **porous silicon**)

L48 ANSWER 4 OF 15 HCA COPYRIGHT 2001 ACS
132:328551 Manufacture of semiconductor wafer involving **etching** of laminated substrates and the manufactured wafer. Sakaguchi, Kiyofumi (Canon Inc., Japan). Jpn. Kokai Tokkyo Koho JP 2000133558 A2 20000512, 10 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1998-300598 19981022.
AB A **porous Si** layer on a wafer in the laminate is removed by **etching** in the process for manufg. a SOI (**silicon** on insulator) **wafer**. A soln. used for the **etching** circulates between a deaerator, preferably a hollow-fiber membrane, and an **etching** vessel. A gas or bubbles are dissolved quickly in the **etching** soln. because the soln. is deaerated enough and **etching** without being disturbed by gas or bubbles can be performed.
IC ICM H01L021-02
CC 76-3 (Electric Phenomena)
ST semiconductor **wafer** laminated **silicon substrate etching**; deaeration **etchant** soln semiconductor wafer manuf; hollow fiber membrane deaeration **etching** soln
IT **Etching**
Semiconductor device fabrication
(deaeration of **etching** soln. for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT Degassing
(deaeration; deaeration of **etching** soln. for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT Membranes, nonbiological
(hollow-fiber; for deaeration of **etching** soln. for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT Buffers
(in **etching** soln. subjected to deaeration for removal

of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT **7664-39-3**, **Hydrofluoric acid**, processes
7722-84-1, **Hydrogen peroxide**, processes
(aq.; deaeration of **etching** soln. for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT 12125-01-8, Ammonium fluoride
(buffer; in **etching** soln. subjected to deaeration for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT 64-17-5, Ethanol, uses
(surfactant; for deaeration of **etching** soln. for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT 67-63-0, Isopropyl alcohol, uses
(surfactant; for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)
IT 67-56-1, Methanol, uses
(surfactant; in **etching** soln. subjected to deaeration for removal of bubbles for manuf. of **silicon** semiconductor **wafer**)

L48 ANSWER 5 OF 15 HCA COPYRIGHT 2001 ACS
129:22211 Manufacturing a semiconductor article. Sakaguchi, Kiyofumi; Yonehara, Takao; Atoji, Tadashi (Canon Kabushiki Kaisha, Japan). Eur. Pat. Appl. EP 843346 A2 19980520, 34 pp. DESIGNATED STATES: R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO. (English). CODEN: EPXXDW. APPLICATION: EP 1997-309196 19971114. PRIORITY: JP 1996-304539 19961115.
AB A method of manufg. a semiconductor article comprises prepg. a 1st **substrate** including a **Si substrate** having a **porous Si** layer and a nonporous semiconductor layer arranged on the **porous Si** layer, bonding the 1st substrate and a 2nd substrate to produce a multilayer structure with the nonporous semiconductor layer located inside, sepg. the 1st and 2nd substrates from each other along the **porous Si** layer by heating the multilayer structure and removing the **porous Si** layer remaining on the sepd. 2nd substrate.
IC ICM H01L021-20
CC 76-3 (Electric Phenomena)
ST semiconductor article manuf; **porous silicon** layer semiconductor article manuf; heating semiconductor article manuf
IT Anodizing
Chemical vapor deposition
Epitaxy
Etching
Laser heating
Thermal oxidation
(in manuf. of a semiconductor article)

IT **7664-39-3**, **Hydrogen fluoride**, processes
(anodizing and **etching** by; in manuf. of a semiconductor article)
IT 64-19-7, Acetic acid, processes 7697-37-2, Nitric acid, processes **7722-84-1**, **Hydrogen peroxide**, processes
(**etching** by; in manuf. of a semiconductor article)

L48 ANSWER 6 OF 15 HCA COPYRIGHT 2001 ACS
129:11682 Fabrication of semiconductor device having semiconductor substrate formed using a porous semiconductor layer, and semiconductor device. Yonehara, Takao; Sato, Nobuhiko; et al. (Canon Kabushiki Kaisha, Japan). U.S. US 5750000 A 19980512, 88 pp. Cont.-in-part of U.S. Ser. No. 551,450, abandoned. (English). CODEN: USXXAM. APPLICATION: US 1996-755356 19961125. PRIORITY: JP 1990-206548 19900803; JP 1991-210369 19910729; JP 1991-210370 19910729; JP 1991-214241 19910801; JP 1991-214242 19910801; JP 1991-214243 19910801; JP 1991-214244 19910801; JP 1991-216573 19910802; JP 1991-216574 19910802; JP 1991-216575 19910802; US 1991-740439 19910805; US 1992-921232 19920729; US 1994-191767 19940204; US 1994-355117 19941213; US 1995-514984 19950814; US 1995-551450 19951101.
AB A semiconductor device having a substrate with an insulating surface and a non-porous semiconductor region bonded to the body of the device. A porous semiconductor region on the surface of the substrate was removed by **etching**.
IC ICM H01L021-00
NCL 156630100
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 74, 75
ST semiconductor device manuf **substrate porous silicon**
IT Alcohols, uses
(**etchant**; fabrication of semiconductor device having semiconductor substrate formed using a epitaxial porous semiconductor layer)
IT **Etching**
Heat treatment
RAM devices
Reactive ion **etching**
(fabrication of semiconductor device having semiconductor substrate formed using a epitaxial porous semiconductor layer)
IT **7664-39-3**, **Hydrofluoric acid**, uses
(anodization soln., **etchant**; semiconductor substrate formed using a epitaxial porous semiconductor layer for semiconductor device fabrication)
IT 64-19-7, Acetic acid, uses 1310-58-3, Potassium hydroxide (KOH), uses 1310-73-2, Sodium hydroxide (NaOH), uses 7697-37-2, Nitric acid, uses **7722-84-1**, **Hydrogen peroxide**, uses
(**etchant**; fabrication of semiconductor device having semiconductor substrate formed using a epitaxial porous semiconductor layer)

L48 ANSWER 7 OF 15 HCA COPYRIGHT 2001 ACS
128:314551 The influence of surface treatment on the optical spectra of **porous silicon**. Ziemianski, P.; Misiewicz, J. (Institute of Physics, Technical University of Wroclaw, Wroclaw, 50-370, Pol.). Electron Technol., 30(3), 277-279 (English) 1997. CODEN: ETNTAT. ISSN: 0070-9816. Publisher: Institute of Electron Technology.

AB **Porous Si wafers** were obtained by electrochem. **etching** in **HF** soln. The change in the photoluminescence spectra for freshly anodized, boiled in H2O and soaked in **H2O2** soln. wafers were studied. The blue-shift of PL spectra for samples boiled in H2O and change in the PL intensity for samples soaked in **H2O2** soln. were obsd. The influence of quantum effect and surface coverage on **porous Si** PL spectra are discussed.

CC 73-5 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)

ST luminescence **surface** spectra **porous silicon**

IT Luminescence
UV and visible spectra
(influence of surface treatment on optical spectra of **porous silicon**)

IT **7440-21-3**, **Silicon**, properties
(**porous**; influence of surface treatment on optical spectra of **porous silicon**)

L48 ANSWER 8 OF 15 HCA COPYRIGHT 2001 ACS
126:165287 Process for producing semiconductor substrate. Yamagata, Kenji; Yonehara, Takao; Sato, Nobuhiko; Sakaguchi, Kiyofumi (Canon K. K., Japan). Eur. Pat. Appl. EP 753886 A1 19970115, 24 pp. DESIGNATED STATES: R: DE, ES, FR, GB, IT, NL, SE. (English). CODEN: EPXXDW. APPLICATION: EP 1996-305134 19960712. PRIORITY: JP 1995-177189 19950713.

AB A process for producing a semiconductor substrate is provided which comprises providing a 1st **substrate** made of **Si** having a **porous Si** layer formed on it by making the substrate porous and a nonporous single-crystal Si layer epitaxially grown on the **porous Si** layer, laminating the 1st substrate onto a 2nd substrate such that the facing surfaces of the 1st and/or the 2nd **substrate** have **Si** oxide layers and the nonporous single-crystal Si layer is interposed between the laminated substrates, and removing the **porous Si** layer by **etching** with an **etchant** which **etches** the nonporous Si layer and the Si oxide layer at .ltoreq.10 .ANG./min.

IC ICM H01L021-306
ICS H01L021-762; H01L021-20

CC 76-3 (Electric Phenomena)

ST **silicon substrate** prodn; **porous** layer **silicon substrate**; silica layer **silicon**

substrate; epitaxial layer **silicon substrate**; lamination **silicon substrate**

IT Alkali metal hydroxides
Bases, processes
(**etching** by; of **porous silicon** in prodn. of semiconductor substrates)

IT Anodizing
(in formation of **porous silicon** in prodn. of semiconductor substrates)

IT **Etching**
(of **porous silicon** in prodn. of semiconductor substrates)

IT 64-19-7, Acetic acid, processes 75-59-2, TMAH **7664-39-3**, **Hydrogen fluoride**, processes 7697-37-2, Nitric acid, processes **7722-84-1**, **Hydrogen peroxide**, processes
(**etching** by; of **porous silicon** in prodn. of semiconductor substrates)

IT 7631-86-9, Silica, processes
(prodn. of **silicon substrates** having layers of)

IT 7440-21-3, **Silicon**, processes
(producing **substrates** from)

L48 ANSWER 9 OF 15 HCA COPYRIGHT 2001 ACS

125:126465 Photoluminescence study of **porous silicon** treated in ultraviolet-irradiated **hydrogen peroxide**. Rao, B.V. Rama Mohana; Basu, P.K.; Biswas, J.C.; Lahiri, S.K. (Microelectronics Centre, Indian Institute of Technology, Kharagpur, India). Proc. SPIE-Int. Soc. Opt. Eng., 2733(Semiconductor Devices), 582-584 (English) 1996. CODEN: PSISDG. ISSN: 0277-786X.

AB The luminescence from **porous Si** films on p-type **Si substrates** of resistivity 7-14 .OMEGA.-cm prepd. by anodic **etching** in 48%**HF**:EtOH(1:1 vol.) is enhanced 390 times by post-anodization treatment in UV irradiated **H2O2**. A small shift of peak wavelength from 750 nm (as-anodized) to 810 nm was obsd. after **H2O2** treatment. The faster oxidn. of **Si surface** in UV irradiated **H2O2** due to the presence of nascent O is believed to cause a more pronounced quantum-size effect responsible for the enhancement of luminescence. The nascent O is expected to prevent H incorporation on the **Si surface**, resulting in a small pos. shift of wavelength due to O incorporation.

CC 73-5 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)

ST luminescence **porous silicon** irradiated **hydrogen peroxide**

IT Size effect
(luminescence of **porous silicon** treated in UV-irradiated **hydrogen peroxide** in relation to)

IT Photolysis
(luminescence of **porous silicon** treated in **hydrogen peroxide** upon)
IT Electric resistance
Etching
Luminescence
(of **porous silicon** treated in UV-irradiated **hydrogen peroxide**)
IT **7722-84-1**, **Hydrogen peroxide**, processes
(luminescence of **porous silicon** treated in UV-irradiated)
IT 7782-44-7, Oxygen, processes
(nascent; luminescence of **porous silicon** treated in UV-irradiated **hydrogen peroxide** in relation to)
IT **7440-21-3**, **Silicon**, properties
(**porous**; luminescence of UV-irradiated **hydrogen peroxide**-treated)

L48 ANSWER 10 OF 15 HCA COPYRIGHT 2001 ACS
124:70444 Large enhancement of photoluminescence from **porous silicon** films by post-anodization treatment in boiling **hydrogen peroxide**. Rama, B. V.; Rao, Mohana; Basu, P. K.; Biswas, J. C.; Lahiri, S. K.; Ghosh, S.; Bose, D. N. (Microelectronics Centre, Indian Inst. Technol., Kharagpur, 721 302, India). Solid State Commun., 97(5), 417-18 (English) 1996. CODEN: SSCOA4. ISSN: 0038-1098.
AB The photoluminescence from **porous Si** films on p-type **Si substrates** of resistivity 12 .omega.-cm prepd. by anodic **etching** in dil. **HF** was greatly enhanced by post-anodization treatment in boiling **H2O2**. A small red shift followed by a slight blue shift was obsd. The formation of ultra-small Si clusters and the oxygenation of the Si-SiO2 interface are believed to be responsible for the above phenomena.
CC 73-5 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
ST luminescence **porous silicon** film **hydrogen peroxide**
IT Luminescence
(large enhancement of photoluminescence from **porous silicon** films by post-anodization treatment in boiling **hydrogen peroxide**)
IT 7631-86-9, Silicon oxide (SiO2), properties **7664-39-3**, **Hydrogen fluoride**, properties **7722-84-1**, **Hydrogen peroxide**, properties
(large enhancement of photoluminescence from **porous silicon** films by post-anodization treatment in boiling **hydrogen peroxide**)
IT **7440-21-3**, **Silicon**, properties
(**porous**; large enhancement of photoluminescence from **porous silicon** films by post-anodization

treatment in boiling **hydrogen peroxide**)

L48 ANSWER 11 OF 15 HCA COPYRIGHT 2001 ACS
123:72210 **Etchants**, **etching** method of **porous Si** and semiconductor **substrates** prepared using thereof. Yonehara, Takao; Sato, Nobuhiko; Sakaguchi, Kiyofumi (Canon K. K., Japan). Jpn. Kokai Tokkyo Koho JP 06342784 A2 19941213 Heisei, 53 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1992-59118 19920214. PRIORITY: JP 1991-42212 19910215; JP 1991-42213 19910215; JP 1991-55601 19910228; JP 1991-55602 19910228; JP 1991-55603 19910228; JP 1991-55604 19910228; JP 1991-55605 19910228; JP 1991-55606 19910228; JP 1991-55607 19910228; JP 1991-55608 19910228; JP 1991-55609 19910228; JP 1991-55610 19910228; JP 1991-55611 19910228; JP 1991-55612 19910228; JP 1991-55613 19910228; JP 1991-55614 19910228; JP 1991-85755 19910327; JP 1991-148160 19910524; JP 1991-148161 19910524; JP 1991-148163 19910524.

AB **Hydrofluoric acid**, buffered **hydrofluoric acid**, and alc., hydroperoxide are mixed for **etching porous Si**. Uniform **etching** of **porous Si** is carried in semiconductor processing with contaminations. In the substrates having both **porous Si** and non-**porous Si**, the **porous Si** is selectively **etched** the disclosed **etchants**.

IC ICM H01L021-308
ICS H01L021-306

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75

ST **porous silicon etching etchant** ; **hydrofluoric acid** alc **hydrogen peroxide etchant**

IT **Etching**
(**etchants**, **etching** method of **porous Si**)

IT Glass, oxide
(**etchants**, **etching** method of **porous Si**)

IT 7440-21-3, Silicon, processes
(**etchants**, **etching** method of **porous Si**)

IT 64-17-5, Ethylalcohol, reactions **7664-39-3**, **Hydrofluoric acid**, reactions **7722-84-1**, **Hydrogen peroxide**, reactions 12125-01-8, Ammonium fluoride
(**etchants**, **etching** method of **porous Si**)

IT 12033-89-5, Silicon nitride, uses
(**etchants**, **etching** method of **porous Si**)

L48 ANSWER 12 OF 15 HCA COPYRIGHT 2001 ACS

120:336083 Epitaxial layer transfer by bond and **etch** back of **porous Si**. Yonehara, Takao; Sakaguchi, Kiyofumi; Sato, Nobuhiko (Semicond. R&D Cent., Tamura, 6770, Japan). Appl. Phys. Lett., 64(16), 2108-10 (English) 1994. CODEN: APPLAB. ISSN: 0003-6951.

AB A novel method for bond and **etch** back Si on insulator in which an epitaxial **Si** layer over **porous Si** is transferred onto a dissimilar substrate by bonding and **etch** back of **porous Si**. The highest **etching** selectivity (100,000:1) between the **porous Si** and the epitaxial layer is achieved by the alkali free soln. of **HF**, **H2O2**, and H2O which is essential for this single **etch**-stop method to produce a submicron-thick active layer with superior thickness uniformity (473.+-.14 nm) across a 5 in. **Si**-on-insulator **wafer**.

CC 76-3 (Electric Phenomena)

ST bonding **etching porous silicon** epitaxial transfer

IT **Etching**
(of **porous silicon**, in epitaxial layer transfer)

IT 7440-21-3, Silicon, miscellaneous
(bonding and **etch** back of porous, in epitaxial layer transfer)

IT **7722-84-1**, **Hydrogen peroxide**, reactions
(**etching** by **hydrofluoric acid** and, of **porous silicon**, in epitaxial layer transfer)

IT **7664-39-3**, **Hydrofluoric acid**, reactions
(**etching** by **hydrogen peroxide** and, of **porous silicon**, in epitaxial layer transfer)

L48 ANSWER 13 OF 15 HCA COPYRIGHT 2001 ACS

119:260790 Preparation of semiconductor device substrates. Sakaguchi, Kiyofumi; Yonehara, Takao (Canon K. K., Japan). Eur. Pat. Appl. EP 554795 A1 19930811, 45 pp. DESIGNATED STATES: R: DE, FR, GB. (English). CODEN: EPXXDW. APPLICATION: EP 1993-101333 19930128. PRIORITY: JP 1992-46306 19920131.

AB At least 1 surface of a 1st **Si substrate** is made porous; the inside walls of the pores are oxidized; a single-crystal Si layer is formed on the **porous Si surface**; the single-crystal Si layer is bonded to 1 surface of a 2nd substrate through a dielec. layer; the 1st substrate is removed, except for the porous layer, by selective **etching**; and selectively removing the porous layer by impregnating the porous layer with **HF**, a mixt. of **HF** and an alc. and/or **H2O2**, buffered **HF**, or a mixt. of buffered **HF** and an alc. and/or **H2O2**.

IC ICM H01L021-84
ICS H01L021-20

CC 76-3 (Electric Phenomena)
ST semiconductor device substrate prepn; **silicon substrate** prepn **etching**; **hydrofluoric acid etching silicon substrate**; alc **hydrofluoric acid etching silicon substrate**; **hydrogen peroxide etching silicon substrate**
IT Alcohols, reactions
(**etching** by **hydrofluoric acid** and, in semiconductor device substrate prepn.)
IT **7722-84-1**, **Hydrogen peroxide**, reactions
(**etching** by **hydrofluoric acid** and, in semiconductor device substrate prepn.)
IT **7664-39-3**, **Hydrofluoric acid**, reactions
(**etching** by, in semiconductor device substrate prepn.)

L48 ANSWER 14 OF 15 HCA COPYRIGHT 2001 ACS
119:239521 **Etching** of **porous silicon** layers in manufacture of semiconductor wafers. Sakaguchi, Kiyofumi; Yonehara, Takao; Sato, Nobuhiko (Canon K. K., Japan). Faming Zhuanli Shenqing Gongkai Shuomingshu CN 1066748 A 19921202, 139 pp. (Chinese). CODEN: CNXXEV. APPLICATION: CN 1992-101589 19920215. PRIORITY: JP 1991-42212 19910215; JP 1991-148164 19910524.
AB Semiconductor wafers are manufd. by forming a Si single-crystal layer on a **porous Si substrate** and a dielec. layer on another substrate, bonding the 2 **substrates** with the **Si** single-crystal layer and the dielec. layer facing each other, and **etching** away the **porous Si substrate** using an **etching** soln. contg. **HF**, EtOH, and **H2O2**.
IC ICM H01L021-302
ICS H01L021-00; C23F001-24
CC 76-3 (Electric Phenomena)
ST semiconductor **wafer etching porous silicon**
IT **Etching**
(of **porous silicon** layers in manufg. **silicon wafers**)
IT Semiconductor devices
(**silicon wafers** for, manuf. of, by **etching** of **porous silicon** layers)
IT 64-17-5, Ethanol, uses **7722-84-1**, **Hydrogen peroxide**, uses
(**etching** soln. contg. **hydrofluoric acid** and, for **porous silicon** layers for manuf. of **silicon wafers**)
IT **7664-39-3**, **Hydrofluoric acid**, uses
(**etching** solns. contg., for **porous silicon** layers for manuf. **silicon wafers**)
IT **7440-21-3P**, **Silicon**, uses

(**wafers**, **etching** of **porous**
silicon layers in manuf. of)

L48 ANSWER 15 OF 15 HCA COPYRIGHT 2001 ACS
119:84075 **Silicon substrate** and method of processing
the same. Sakaguchi, Kiyofumi; Yonehara, Takao (Canon K. K.,
Japan). Eur. Pat. Appl. EP 534474 A2 19930331, 56 pp. DESIGNATED
STATES: R: DE, FR, GB. (English). CODEN: EPXXDW. APPLICATION: EP
1992-116486 19920925. PRIORITY: JP 1991-275053 19910927; JP
1991-275052 19910927; JP 1991-275054 19910927; JP 1991-276375
19910930; JP 1991-276374 19910930; JP 1991-276376 19910930.

AB A Si product suitable for use in, e.g., semiconductor devices or X-ray masks, is produced by a process having the steps of prepg. a nonporous **Si substrate**, changing by anodization at least a portion of the **substrate** into **porous Si** thereby forming **porous Si** region penetrating the substrate from one to the other side thereof, and **etching** the substrate by using an **etchant** contg. **HF** so as to remove the **porous Si** region. The substrate may be provided with an **etching** stop layer. In such a case, an unsupported membrane region formed by the **etching** stop layer is left after the removal of the **porous Si** region.

IC ICM H01L021-76
ICS H01L021-20; H01L021-306

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 72, 73

ST processed **silicon substrate** semiconductor
device; x ray mask processed **silicon substrate**;
anodization **etching silicon substrate**

IT Semiconductor devices
(anodization and **etching** of **silicon**
substrates for)

IT Alcohols, uses
(in **etching** anodized **silicon**
substrates)

IT **Etching**
(of anodized **silicon substrates**, for
semiconductor devices and x-ray masks)

IT Anodization
(of **silicon substrates**, with subsequent
etching)

IT Photomasks
(x-ray, anodization and **etching** of **silicon**
substrates for)

IT 7647-01-0, Hydrochloric acid, uses **7722-84-1**,
Hydrogen peroxide, uses
(in **etching** anodized **silicon**
substrates)

IT **7440-21-3**, **Silicon**, reactions
(**substrates**, anodization and **etching** of)

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L49 ANSWER 1 OF 17 HCA COPYRIGHT 2001 ACS
135:337941 Method for gate-drain multilayer structure by liquid phase deposition of silica layer in CMOS fabrication. Wu, Shie-Lin (Powerchip Semiconductor Corporation, Taiwan). Taiwan TW 383408 B 20000301, 22 pp. (Chinese). CODEN: TWXXA5. APPLICATION: TW 1997-86104000 19970328.

AB A method for CMOS transistor multilayer gate-drain structure is disclosed. A field oxide layer is formed on a semiconductor substrate, followed by 1st conductive well, 2nd conductive well, gate electrode and gate oxide layer. A first dielec. layer is formed on top of gate electrode and gate oxide layer to compensate damaged gate oxide layer, followed by a lightly doped drain electrode formation in the 1st conductive well and 2nd conductive well. A plurality of amorphous Si sidewall is formed on both sides of the gate electrode, followed by formation of heavily doped source/drain electrodes and gate electrodes. A liq. phase deposited silicon oxide sidewall is formed on both sides of amorphous Si sidewall. and metal silicide is formed on source/drain electrodes, gate electrode and amorphous Si sidewall which are not covered with on liq. phase deposited Si oxide sidewall. Finally, metal silicide is formed on source/drain electrodes, gate electrode and amorphous Si sidewall which are not covered with on liq. phase deposited Si oxide sidewall.

IC ICM H01L021-28

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75

IT **Etching**
(anisotropic; multilayer gate-drain structure by liq. phase deposition of silica layers in CMOS fabrication)

IT Sputtering
(**etching**, reactive; multilayer gate-drain structure by liq. phase deposition of silica layers in CMOS fabrication)

IT **Etching**
(sputter, reactive; multilayer gate-drain structure by liq. phase deposition of silica layers in CMOS fabrication)

IT **Oxidation**
(thermal, silicon substrate; multilayer gate-drain structure by liq. phase deposition of silica layers in CMOS fabrication)

IT **7440-21-3**, Silicon, processes
(amorphous, substrate; multilayer gate-drain structure by liq. phase deposition of silica layers in CMOS fabrication)

IT 7429-90-5, Aluminum, processes **7664-39-3**, **Hydrogen fluoride**, processes 10043-35-3, Boric acid, processes 16961-83-4, Hydrogen hexafluorosilicate (H2SiF6)
(liq. phase deposition; multilayer gate-drain structure by liq. phase deposition of silica layers in CMOS fabrication)

IT 11104-62-4, Cobalt silicide 11129-80-9, **Platinum** silicide 12039-83-7, Titanium disilicide

(**multilayer** gate-drain structure by liq. phase deposition of silica layers in CMOS fabrication)

L49 ANSWER 2 OF 17 HCA COPYRIGHT 2001 ACS
135:99755 Design and fabrication of silicon micro-bench with V groove for coupling. Yang, Chenghui (Chongqing Optoelectronics Research Institute, Chungking, 400060, Peop. Rep. China). Bandaoti Guangdian, 21(Suppl.), 73-74 (Chinese) 2000. CODEN: BAGUE5. ISSN: 1001-5868. Publisher: Bandaoti Guangdian Bianjibu.
AB The design and manuf. of high quality Si V-groove for coupling of $LiNbO_3$ integrated optical devices were introduced. The manuf. process comprised polishing Si wafer, **oxidizing**, photoetching, and **etching** at 78.degree. by using a mixt. of KOH, isopropanol, and H_2O (1:2:2). The photoetching process comprised depositing a layer of Cr and a **layer** of **Au** (80 nm) by evapn. on **oxidized** Si wafer, **etching** Cr and Au by using photoresist as mask, **etching** SiO_2 by using Cr and Au as masks by using a mixt. of **HF**, NH_4F, and H_2O (1:2:3), and removing photoresist, Cr, and Au.
CC 74-11 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
IT Evaporation
Optics
Oxidation
Photoresists
(design and fabrication of silicon micro-bench with V groove for coupling)
IT **Etching**
(photochem.; design and fabrication of silicon micro-bench with V groove for coupling)
IT **7440-21-3**, Silicon, processes 7440-47-3, Chromium, processes 7440-57-5, Gold, processes
(design and fabrication of silicon micro-bench with V groove for coupling)
IT 67-63-0, Isopropanol, uses 1310-58-3, Potassium hydroxide, uses **7664-39-3**, **Hydrofluoric acid**, uses
12125-01-8, Ammonium fluoride
(design and fabrication of silicon micro-bench with V groove for coupling)

L49 ANSWER 3 OF 17 HCA COPYRIGHT 2001 ACS
134:246234 Eliminating buried contact trench in MOSFET devices having self-aligned silicide. Wu, Shye-Lin (Texas Instruments - Acer Incorporated, Taiwan). U.S. US 6211556 B1 20010403, 11 pp., Cont.-in-part of U.S. Ser. No. 65,323. (English). CODEN: USXXAM. APPLICATION: US 1999-323773 19990601. PRIORITY: US 1998-65323 19980423.
AB A MOSFET device with buried contact structure on a semiconductor substrate has the following major elements with their relative locations. A gate insulator is on a portion of the substrate and a gate electrode is on the gate insulator. A gate sidewall structure

is located on side-walls of the gate electrode. Inside the substrate, a lightly doped source/drain region is under the gate sidewall structure, and a doped source/drain region is abutting the lightly doped source/drain region and located aside from a region under the gate sidewall structure. In addn., a doped buried contact region is also in the substrate next to the doped source/drain region. On the substrate, a Si connection is located on a portion of the doped buried contact region, and a shielding block is on the doped buried contact region covering only a region uncovered by the Si connection. Specifically, the shielding block includes dielec. side-walls and Si side-walls and the shielding block is formed right next to the edge of the Si connection.

IC ICM H01L029-76
ICS H01L029-94; H01L031-062; H01L031-113; H01L031-119
NCL 257382000
CC 76-3 (Electric Phenomena)
IT Sputtering
(**etching**, reactive, buried contact opening formation; eliminating buried contact trench in MOSFET devices having self-aligned silicide)
IT **Etching**
(sputter, reactive, buried contact opening formation; eliminating buried contact trench in MOSFET devices having self-aligned silicide)
IT **Oxidation**
(thermal; eliminating buried contact trench in MOSFET devices having self-aligned silicide)
IT 7440-02-0, Nickel, processes 7440-06-4, **Platinum**, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7440-47-3, Chromium, processes 7440-48-4, Cobalt, processes
(metal **layer** deposition on Si connections; eliminating buried contact trench in MOSFET devices having self-aligned silicide)
IT **7440-21-3**, Silicon, processes
(substrate, connections; eliminating buried contact trench in MOSFET devices having self-aligned silicide)
IT 7664-38-2, Phosphoric acid, uses **7664-39-3**, **Hydrofluoric acid**, uses
(wet **etching**; eliminating buried contact trench in MOSFET devices having self-aligned silicide)

L49 ANSWER 4 OF 17 HCA COPYRIGHT 2001 ACS
133:186471 Improved method for depositing semiconductor thin films on porous structures in semiconductor device fabrication. Tayanaka, Hiroshi (Sony Corp., Japan). U.S. US 6107213 A 20000822, 48 pp., Cont.-in-part of U.S. 5,811,348. (English). CODEN: USXXAM. APPLICATION: US 1997-818239 19970314. PRIORITY: US 1996-595382 19960201; JP 1996-61552 19960318; JP 1996-234480 19960904.
AB The present invention provides new and improved methods for making cryst. semiconductor thin films which may be bonded to different kinds of substrates. The thin films may be flexible. In accordance

with preferred methods, a multilayer porous structure including two or more porous layers having different porosities is formed in a semiconductor substrate. A semiconductor thin film is grown on the porous structure. Electrodes and/or a desired support substrate may be attached to the grown film. The grown film is sepd. from the semiconductor substrate along a line of weakness defined in the porous structure. The sepd. thin film attached to the support substrate may be further processed to provide improved film products, solar panels and light emitting diode devices. These thin film semiconductors are excellent in crystallinity and may be inexpensively produced, thereby enabling prodn. of solar cells and light emitting diodes at lower cost.

IC ICM H01L021-20
NCL 438762000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 52, 73
IT Adhesive bonding
Annealing
Contact holes
Dielectric films
Electric contacts
Electrolytic cells
Etching
Interconnections (electric)
Lamination
Photolithography
Printed circuit boards
(in improved method for depositing semiconductor thin films on porous structures in semiconductor device fabrication)
IT Anodization
Oxidation
(of porous layer; in improved method for depositing semiconductor thin films on porous structures in semiconductor device fabrication)
IT **7664-39-3**, **Hydrogen fluoride**, processes
(electrolytic soln.; in improved method for depositing semiconductor thin films on porous structures in semiconductor device fabrication)
IT **7440-05-3**, **Palladium**, processes 7440-22-4, Silver, processes 7440-32-6, Titanium, processes
(**film**; in improved method for depositing semiconductor thin films on porous structures in semiconductor device fabrication)
IT **7440-21-3**, Silicon, processes
(substrate; improved method for depositing semiconductor thin films on porous structures in semiconductor device fabrication)

L49 ANSWER 5 OF 17 HCA COPYRIGHT 2001 ACS
132:200495 Electroluminescence (EL) from photo-chemically **etched** silicon. Yamamoto, N.; Sumiya, A.; Takai, H. (Department of Electrical Engineering, Tokyo Denki University, Chiyodaku, Tokyo, Japan). Mater. Sci. Eng., B, B69-70, 205-209 (English) 2000.

CODEN: MSBTEK. ISSN: 0921-5107. Publisher: Elsevier Science S.A..

AB Luminescence from Si-based materials was studied to develop new opto-electronic devices on a Si wafer. The authors propose a photo-chem. **etching** method to form a luminescent layer on a Si wafer. A comparison between electroluminescence (EL) and luminescence from the photo-chem. **etched** Si is discussed. In the photo-chem. **etching** method, a Si wafer (100) with resistivity of 35-45 or 0.22-0.38 .OMEGA.-cm is set at the bottom of a vessel filled with an **etchant** (**HF** + **H2O2**), and a He-Ne laser (633 nm, 18.4 mW/cm2) is irradiated onto the surface for 30 min. An **Au** thin **film** (thickness 5 nm) is deposited onto the **etched** **layer**, and a **Au**-Sb (1%) **film** is deposited on the reverse side of the Si wafer to form ohmic contacts. The EL from the **etched** layer is obsd. by applying a voltage at -30 - .apprx.30V to the electrodes. Luminescence from the **etched** layer is measured by He-Cd laser excitation (325 nm). The peak wavelength of EL at forward bias coincides with a peak wavelength of luminescence. EL spectra at backward bias can be fitted by 2 Gaussian functions, and one of them coincides with a peak wavelength of luminescence. The EL from the photo-chem. **etched** Si can be explained schematically by an elec. circuit model.

CC 73-5 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 76

ST silicon photochem **etching** luminescence electroluminescence

IT Electric circuits
(electroluminescence of photo-chem. **etched** silicon explained by)

IT Optoelectronics
(electroluminescence of photo-chem. **etched** silicon in relation to)

IT Luminescence, electroluminescence
(of photo-chem. **etched** silicon)

IT Electric current-potential relationship
Luminescence
(of photo-chem. **etched** silicon in relation to electroluminescence)

IT **Etching**
(photochem.; electroluminescence of photo-chem. **etched** silicon)

IT **7440-21-3**, Silicon, properties
(electroluminescence of photo-chem. **etched** silicon)

L49 ANSWER 6 OF 17 HCA COPYRIGHT 2001 ACS

126:321663 Palladium-promoted **oxidation** of Si at low temperatures. Kobayashi, H.; Kawa, H.; Yuasa, T.; Nakato, Y.; Yoneda, K. (PRESTO, Research Development Corporation of Japan, Higashi-Hiroshima, 739, Japan). Appl. Surf. Sci., 113/114, 590-594 (English) 1997. CODEN: ASUSEE. ISSN: 0169-4332. Publisher: Elsevier.

AB A **palladium** (**Pd**) **layer** deposited on the ultrathin silicon oxide-covered Si substrate promotes Si **oxidn**. Take-off angle dependent XPS measurements and the capacitance-voltage measurements show that after the heat treatment of the .ltbbrac.Pd/chem. oxide/Si(100).rtbbrac. specimens at 400.degree.C in oxygen, the thickness of the oxide **layer** between the **Pd layer** and the Si substrate increases to 4-4.5 nm but no oxide is formed on the Pd surface. When the **Pd layer** is deposited on the **hydrofluoric acid-etched** Si surface, palladium silicide is formed, while no silicide is formed in cases where the **Pd film** is deposited on the thin chem. oxide covered-Si substrate. It is concluded that the diffusing and reaction species are oxygen atoms (or oxygen ions), initially formed at the Pd surface.

CC 67-3 (Catalysis, Reaction Kinetics, and Inorganic Reaction Mechanisms)

ST palladium promoted **oxidn** silicon low temp

IT **Oxidation**
Oxidation catalysts
(palladium-promoted **oxidn**. of Si at low temps.)

IT 7440-05-3, Palladium, uses
(palladium-promoted **oxidn**. of Si at low temps.)

IT **7440-21-3**, Silicon, reactions
(palladium-promoted **oxidn**. of Si at low temps.)

L49 ANSWER 7 OF 17 HCA COPYRIGHT 2001 ACS

126:205974 Differences between N and P-type substrates in the platinum deposition on silicon. Gorostiza, Pau; Diaz, Rauel; Sanz, Fausto; Morante, Joan Ramon (Dep. Quimica Fisica, Univ. Barcelona, Barcelona, E-08028, Spain). Proc. - Electrochem. Soc., 96-19(Electrochemically Deposited Thin Films), 125-135 (English) 1997. CODEN: PESODO. ISSN: 0161-6374. Publisher: Electrochemical Society.

AB Platinum electroless deposition on silicon from **HF** solns. is studied by SEM and TEM, focusing on the different behavior of n and p-type samples. In both cases the silicon substrate is **etched** while platinum nucleates on the surface, and a complete **platinum layer** is eventually formed. The process seems to be hindered on n substrates and displays a more local behavior compared to p substrates. The results are discussed in terms of a global electrochem. redox reaction in which silicon is **oxidized** and platinum reduces injecting holes to the silicon valence band.

CC 76-3 (Electric Phenomena)

ST nitrogen substrate platinum deposition silicon **oxidn**

IT Crystal nucleation
Electrochemical redox reaction
Electroless plating
Etching
Oxidation
Valence band

(differences between N and P-type substrates in platinum deposition on silicon)

IT 7440-06-4, Platinum, properties **7440-21-3**, Silicon, properties
(differences between N and P-type substrates in platinum deposition on silicon)

L49 ANSWER 8 OF 17 HCA COPYRIGHT 2001 ACS

126:97284 Manufacture of gold single crystal thin film with **etching** of substrate. Morikawa, Juko; Ikeda, Tsutomu (Canon Kk, Japan). Jpn. Kokai Tokkyo Koho JP 08306645 A2 19961122 Heisei, 4 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1995-109603 19950508.

AB The title method involves the following steps; **etching** a substrate, depositing a Au single crystal thin film from a supersatd. Au complex soln., and growing. The **Au film** is useful for semiconductor integrated circuits, magnetic circuits, piezoelec. devices, etc. A **Au** thin **film** with large particle size showed good adhesion to substrates.

IC ICM H01L021-285
ICS H01L021-285

CC 75-1 (Crystallography and Liquid Crystals)

ST **gold film** deposition **etching** substrate; single crystal **gold film** **etching** substrate

IT Crystal growth
Etching
(manuf. of gold single crystal thin film with **etching** of substrate)

IT Glass
(substrate; manuf. of gold single crystal thin film with **etching** of substrate)

IT 7440-32-6, Titanium, processes 50926-11-9, ITO
(coating for substrate; manuf. of gold single crystal thin film with **etching** of substrate)

IT **7664-39-3**, **Hydrofluoric acid**, uses
7664-93-9, Sulfuric acid, uses **7722-84-1**, **Hydrogen peroxide**, uses 7738-94-5, Chromic acid (H_2CrO_4)
7782-44-7, Oxygen, uses
(**etchant**; manuf. of gold single crystal thin film with **etching** of substrate)

IT 7440-57-5, Gold, processes
(manuf. of gold single crystal thin film with **etching** of substrate)

IT **7440-21-3**, Silicon, processes
(substrate; manuf. of gold single crystal thin film with **etching** of substrate)

L49 ANSWER 9 OF 17 HCA COPYRIGHT 2001 ACS

121:168419 Manufacture of semiconductor device having electric insulator **film** on **gold**-based circuit showing improved

adhesion. Kuryama, Atsushi (Nippon Electric Co, Japan). Jpn. Kokai Tokkyo Koho JP 06084905 A2 19940325 Heisei, 4 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 1992-134554 19920527.

AB The title device is manufd. by a process including following successive steps; (1) forming an Ag-based circuit on a semiconductor device on a substrate, (2) depositing a Si film on the wafer, (3) forming an alloy from the Ag and the Si under plasma CVD or heating, and (4) forming an elec. insulator film. In the process, (a) the Si film may be formed by sputtering, vapor deposition, or CVD, (b) the plasma CVD for alloying may include initial flow of an **oxidn**. gas, e.g., N2O, O, and the residual Si may be **oxidized**, and (c) the alloy may be formed at 150-400.degree. and the residual Si is removed by **HF**-HNO3-based **etchant**.

IC ICM H01L021-3205
ICS H01L021-316

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 56

IT **Etching**
(removal of residual silicon after alloying with gold-based circuit by, for semiconductor device)

IT **7440-21-3**, Silicon, uses
(alloying of gold-based elec. circuit by, for formation of elec. insulator, for semiconductor device)

IT **7664-39-3**, Fluoric acid, uses 7697-37-2, Nitric acid, uses
(**etchant**, for removal of residual silicon after alloying of gold-based circuit, for semiconductor device)

IT 7782-44-7, Oxygen, reactions 10024-97-2, Nitrogen oxide (N2O), reactions
(**oxidn**. of residual silicon after alloying gold-based circuit by, for semiconductor device)

L49 ANSWER 10 OF 17 HCA COPYRIGHT 2001 ACS

98:41047 Effect of the oxide layer on radiational-stimulated diffusion in silicon. Narkulov, A. (Inst. Yad. Fiz., Tashkent, USSR). Dokl. Akad. Nauk Uzb. SSR (4), 28-30 (Russian) 1982. CODEN: DANUAO. ISSN: 0366-8614.

AB The effect was studied of intermediate SiO2 **films** between **Au** and Si on the diffusion of Au into Si during 60Co x-ray irradn. The oxide films were prepd. by **oxidn**. and **etching**. As the oxide film increases, the amt. of diffusion is reduced.

CC 65-6 (General Physical Chemistry)
Section cross-reference(s): 71, 76

ST diffusion **gold** silica **film** silicon; gamma induced gold diffusion silicon

IT **Etching**
(of silicon, oxide **layer** from, **gold** diffusion through)

IT **7440-21-3**, properties
(diffusion of gold into, through silica layer, .gamma.-ray-induced)

IT **7664-39-3**, reactions

(**oxidn**. of silicon surface by, gold diffusion through
silica layer in relation to)

L49 ANSWER 11 OF 17 HCA COPYRIGHT 2001 ACS
87:203450 A field effect gas sensor for hydrogen. Plihal, Manfred
(Forschungslab., Siemens. A.-G., Munich, Ger.). Siemens Forsch.-
Entwicklungsber., 6(1), 53-9 (German) 1977. CODEN: SFEBBL.
AB The performance curves of a device, consisting of an n-Si disk, a
SiO_2 coating (thickness 35-130 nm, formed by **oxidn**. of the
Si disk at 1100.degree. by wet O_2 and **etching** by dil.
HF), 375 .mu. square **Pd layers**
(thickness 100 nm), and Al point contacts (thickness 100 nm, diam.
100 .mu.), show that it is suitable for detg. H_2 in gases.
CC 47-7 (Apparatus and Plant Equipment)
Section cross-reference(s): 76, 79
IT Semiconductor devices
(silicon, with silica and **palladium coatings**
for hydrogen detn.)
IT 1333-74-0, analysis
(detn. of, semiconductor device with **palladium**
coating for)
IT **7440-21-3**, uses and miscellaneous
(devices, with silica and **palladium coatings**
for hydrogen detn.)

L49 ANSWER 12 OF 17 HCA COPYRIGHT 2001 ACS
77:11104 Method to prepare semiconductor surface barrier nuclear
detectors. Balcarcel, R.; Fernandez, A.; Gallardo, R. (Program
Instrum., Com. Nac. Energ. Nucl., Mexico D. F., Mex.). Rev. Mex.
Fis., 20(Supl.), 55-65 (English) 1971. CODEN: RMXFAT.
AB The advantages, applications, and prepn. of semiconductor detectors
are described. The detectors are prepd. from high-resistivity Si
disks. After washing to remove dust, metallic impurities, and
grease, the disks were **etched** with **HF** soln.,
washed, and then immersed in $Na_2Cr_2O_7$ to **oxidize** the
surface. The disks were then mounted and after masking, a
layer of **Au** was evapd. onto one face and Al evapd.
onto the other. These metallic layers formed the plates of a
capacitor. The characteristics of these detectors are as good as
those of their com. equivs.
CC 71-13 (Electric Phenomena)
Section cross-reference(s): 76
IT **7440-21-3**, uses and miscellaneous
(radiation detectors, surface-barrier)

L49 ANSWER 13 OF 17 HCA COPYRIGHT 2001 ACS
75:114135 Preparation of ohmic contacts on silicon. Amouroux, Claude;
Peres, Gerard; Vallette, Pierre (Compagnie Generale d'Electricite).
Ger. Offen. DE 2104804 19710819, 15 pp. (German). CODEN: GWXXBX.
PRIORITY: FR 19700209.
AB A process is described for the depassivation of a metal to be
etched by coating it with an **oxidizable** metal and

used for the prepn. of an ohmic contact on Si. Thus, a Si plate is coated with a Si oxide layer into which a window corresponding to the contact zone is **etched** by photolithog. The sample is dipped quickly into dil. **HF**, washed in deionized H2O, dried in N, coated with a 500 .ANG. thick **Pt layer** by cathode sputtering and heated 15 min at 500.degree. to give a Pt-Si alloy in the window. The residual Pt is removed with aqua regia in an ultrasound bath. The plate is subsequently coated by cathode sputtering with a Ti and **Pt layer** of 500 and 1000 .ANG. thickness, resp. The **Pt layer** is confined to a region including the contact zone by **coating** the **Pt layer** and the synthetic resin protective layer with a Ag layer by cathode sputtering, treating the Ag 10 sec with dil. HNO3 and **etching** the Pt depassivated by the Ag 6 min in aqua regia. The Ti surface surrounding the Ag is coated with a synthetic resin **layer** and the **Pt layer** is electroplated with a 3 .mu. thick **Au layer**. The layers of synthetic resin and Ti outside of the contact zone are removed and a Au wire is welded to the **Au layer**.

IC C23F; B41C; H01L

CC 71 (Electric Phenomena)

ST silicon Ohmic contact; platinum depassivation silver; **etching** platinum chloroazotic acid

IT **Etching**
(of platinum for contacts on silicon, silver depassivation layers in)

IT Electric contacts
(platinum **etching** for, on silicon, silver depassivation layers in)

IT **7440-21-3**, uses and miscellaneous
(elec. contacts to, silver layers in **etching** of platinum for)

IT 7440-06-4, reactions
(**etching** of, for elec. contacts on silicon, silver layers in depassivation for)

IT 7440-22-4, uses and miscellaneous
(platinum depassivation with, in **etching** for elec. contacts on silicon)

L49 ANSWER 14 OF 17 HCA COPYRIGHT 2001 ACS

74:26188 Monolithic integrated structure. Feinberg, Irving; Langdon, Jack L.; Sitler, Carl L. (International Business Machines Corp.). U.S. US 3539876 19701110, 51 pp. (English). CODEN: USXXAM. APPLICATION: US 19670523.

AB An improved monolithic semiconductor master slice structure is provided for use in making monolithic integrated logic chips that can be readily mounted onto a module. A p-type wafer of 10-20 ohm-cm resistivity, 10 mils thick, is the starting substrate. The substrate has a crystallographic orientation of 2.5.degree. off the .ltbbrac.111.rtbbrac. plane in the direction of the .ltbbrac.110.rtbbrac. plane to minimize pattern shift or washout after epitaxial growth. A 6000-.ANG.-thick SiO2 coating is

deposited or grown on the surface, and a photoresist layer is deposited on the oxide layer. By using an appropriate mask, surface regions are exposed by a buffered **HF** soln. and the photoresist layer is then removed. N+ regions having a concn. of 2 .times. 1020/cm3 are diffused into the exposed portions. The surface oxide layer serves as a diffusion mask. After diffusion, an **oxidn**. is performed to convert the n+ surface regions into oxide, thereby coating a depression on each n+ surface region for location after epitaxial growth. The oxide layer is removed, and an n-type region is epitaxially grown over the entire surface. This region is an As-doped layer 5.5 .mu. thick. The depressions are now located on the surface of the epitaxial layer to facilitate subsequent operations. A 4000-.ANG. oxide layer is formed on the surface of the epitaxial region. An isolation pattern of channels is formed in the oxide layer by standard masking and **etching** . A p+ diffusion is carried out to form isolating p+ regions and a p+ underpass region in the n-type epitaxially grown region. The p+ regions have a low-resistivity surface region which extends downward from the surface and each p+ region extends continuously from the p-substrate region to the structure surface. A reoxidn. is carried out and holes are opened in the oxide layer to permit a base of p-type diffusion for each transistor, p-type resistivity regions for each resistor, and p++ regions for the underpass conductor. This is followed by a simultaneous reoxidn. and drive-in operation. Another SiO2 layer is grown on the substrate surface. The p-type impurities are redistributed, increasing junction depth and lowering the surface concn. A photoresist coating is applied and openings are formed in the oxide layer to permit n+ emitter-type regions to be formed. The 2 n+ contact regions for each collector of the transistor reduces the series resistance of the collector. N+ emitter regions are formed in the p-type base region of each transistor. A phosphosilicate glass layer is formed on the surface due to the P diffusion operation. The base channel width of each transistor is 17 .mu.in due to "push-out" of the base region after formation of the diffused emitter region. The emitter and base regions of each transistor are formed over the buried n+ region to permit this region to act as a buried low-resistivity subcollector. A drive-in operation is carried out using a N atm. This is followed by deposition of a sputtered glass layer on the phosphosilicate glass layer. Contact holes are opened in the oxide layer in selected areas by masking and **etching**. A layer of Al or Mo is evapd. over the entire surface, and portions of this layer are **etched** away to produce the desired interconnection pattern. A layer of photoresist is applied, exposed, developed, and fixed. The interconnections are formed by substractive **etching**. The photoresist is then stripped off and the wafers are sintered in N at 450.degree. for 15 min to permit the Al to produce good ohmic contacts to the regions of the wafer. A layer of SiO2 is formed over the entire surface and openings are formed over the terminal portion of each land that is selected for pad formation. Successive layers of Cr, Cu, and Au are deposited into and about the periphery of each opening formed. Then a layer of Pb-Sn solder is deposited

over each **Au layer** of each terminal hole and a ball of solder is formed on the Au limiting land. Thus, pads of the master slice are formed to permit elec. contact between devices, through the lands, to the module. The specific fabrication steps used in making each semiconductor component employed in each master slice are described in detail.

IC H02B; H05K
NCL 317101000
CC 71 (Electric Phenomena)
IT **7440-21-3**, uses and miscellaneous
(elec. integrated circuits, monolithic)

L49 ANSWER 15 OF 17 HCA

71:86079 Reduction of carrier lifetime in semiconductor device. Castrucci, Paul P.; Hess, Martin S.; Pecoraro, Raymond P. (International Business Machines Corp.). Brit. GB 1161351 19690813, 5 pp. (English). CODEN: BRXXAA. PRIORITY: US 19660331.

AB A method is described for reducing carrier lifetime by injecting carrier-lifetime killers into the semiconductor device in a nonoxidizing atm. after a final oxide layer has been formed on a surface of the device, E.g., an initial SiO2 layer is thermally grown on a p-type Si single-crystal wafer having a resistivity of 10-20 ohm-cm. A photoresist layer is deposited on the wafer, and by using the photoresist layer as a mask, surface regions are exposed by **etching** away the desired portions of the SiO2 layer with a buffered **HF** soln. The photoresist layer is then removed. n-Type impurities are diffused into the exposed surface portions to form n+ regions in the wafer having a concn. of n-type majority carriers of 2 .times. 1020/cc. The oxide layer serves as a mask to prevent an n+ region from being formed across the entire surface. After removing the oxide layer, a region of n-type cond. is epitaxially grown on the wafer surface. The n-type region is an As-doped layer 5.5-6.5 .mu. thick. A 2nd oxide layer is formed on the surface of the epitaxially grown region by thermal **oxidn** ., by pyrrolytic decompn., or by radio-frequency sputtering. A no. of openings are formed in specific areas of the oxide layer by standard techniques. A p-type diffusion step is carried out, using a B source, to form p+ regions in the n-type epitaxially grown layer. In forming isolation diffusions, the diffused p+-type regions reach and become continuous with the p-type original substrate. A 3rd oxide layer is then formed by thermal **oxidn**. A photoresist coating is applied to the surface, and by standard techniques, desired portions of SiO2 layer are removed. A base or resistor diffusion is carried out, using B as the impurity source. This diffusion forms p-type regions having an impurity surface concn. of 5 .times. 1019/cc. This is followed by a reoxidn. drive-in operation. A 4th layer of SiO2 is grown on the base and (or) resistor regions. During this treatment, the B impurities are redistributed, increasing the junction depth and lowering the surface concn. The **oxidn**. drive-in cycle is 25 min. in dry O and 10 min. in steam, followed by 15 min. in dry O at 1150.degree.. In forming transistor devices, a photoresist coating

is applied over the 4th oxide layer and by known methods, portions of this layer are removed over the diffused base regions to permit emitter regions to be formed by diffusion. n-Type emitter regions are formed in the p-type base regions by using a P impurity source (POCl3) and heating the wafer in an atm. contg. 700 ppm. POCl3 at 970.degree. for 35 min. The emitter and base regions are formed over the buried n+ region to permit this region to act as a low-resistivity subcollector. A final **oxidn**. and emitter drive-in operation is formed, using a 5-min. dry O, 55-min. steam cycle followed by dry O heat treatment at 970.degree.. During this heat treatment, a final oxide layer is formed on the semiconductor surface. Carrier lifetime killers are injected into the wafer through an opening in the oxide in the back side of the wafer. A **layer** of **Au** is evapd. on the wafer, and Au is diffused into the structure by heating at 1000.degree. for 20 min. in a nonoxidizing atm. (N). The diffusion is followed by an annealing cycle at 560.degree. for 2 hrs. in N, which also serves to increase the transistor current gain.

IC H01L
CC 71 (Electric Phenomena)
IT **7440-21-3**, uses and miscellaneous
(devices, current carrier lifetime redn. in)

L49 ANSWER 16 OF 17 HCA
68:63756 Applying metallic coatings. Chuss, John T. (Western Electric Co., Inc.). Fr. FR 1486263 19670623, 5 pp. (French). CODEN: FRXXAK. PRIORITY: US 19650709.

AB A metal coating is applied to an area of a substrate surface after treating the substrate to impart a layer of oxide over the rest of the surface, depositing a porous film of a catalytic metal over the entire surface, treating the surface with a solvent capable of selectively dissolving only the oxide, and allowing just enough oxide to dissolve to remove the film of catalyst from the oxide layer. When metal is then deposited from an electroless plating soln., the coating forms only on the catalyst in the desired area. Thus, the surface of a Si (n-type) wafer is **oxidized**, masked, **etched** to expose an area of substrate, then doped with B (p-type). The oxides which form during the B diffusion are removed with a 2:1 mixt. of NH4F and **HF**. The wafer is dipped in an acid SnCl2 soln. to sensitize the surface, then in an acid PdCl2 soln. to activate the Sn film. Rinsing with deionized water follows each dip. Dip times are very short, .apprx.60 and 20-30 sec., resp., to insure the formation of a porous Sn-**Pd** catalyst **film** on the SiO2. A 2nd treatment with NH4F-**HF** floats the catalyst from the oxide layer in 5-7 sec. Finally, Ni is deposited over the catalyst film on the doped area of the wafer from a conventional NiCl2 electroless plating soln. Addnl. coatings of metal and (or) noble metals can be deposited by standard procedures. The product is a diode with a uniform, firmly adhering metal coating on the p-type Si.

IC H01L
CC 71 (Electric Phenomena)

IT Electric contacts
(to silicon devices, deposition of nickel on **palladium** -tin **films** in manuf. of)
IT **7440-21-3P**, uses and miscellaneous
(devices, elec. contacts to, deposition of nickel in manuf. of)

L49 ANSWER 17 OF 17 HCA COPYRIGHT 2001 ACS
67:27152 Gold diffusivities in silicon dioxide and silicon using the metal-oxide- semiconductor structure. Collins, Dean Robert; Schroder, D. K.; Sah, Chih-Tang (Univ. of Illinois, Urbana, Ill., USA). Appl. Phys. Lett., 8(12), 323-5 (English) 1966. CODEN: APPLAB.
AB The (111) Czochralski-grown Si single crystals were n-type, P doped, and lapped to a thickness of 400 .mu.. After **etching** in **HF**:HNO3, the slices were **oxidized**, the oxide removed from one side, and 5000 A. of 6N Au deposited on this side. Au diffusion was performed in dry Ar. In a figure the voltage shifts, .DELTA.V, of the concn.-voltage curves are shown as a function of time and temp. A rapid initial rise followed a more gradual change. The voltage shift is explained. In the region which is controlled by Au diffusion in the SiO2 film, it is assumed that the Au diffusion profile in SiO2 is given by the complementary error function and that the Si-SiO2 boundary acts as a const. source of Au. The surface concn. is relatively temp. independent. Au diffuses in a neg. charged ionic state in both Si and SiO2. Diffusion takes place primarily through the bulk of the Si slice rather than along the bare Si or Si-SiO2 surface.
CC 71 (Electric Phenomena)
IT 7631-86-9, properties
(diffusion of **gold** in **films** of, on silicon)
IT **7440-21-3**, properties
(diffusion of **gold** in silica-**coated**)

=> d l50 1-12 cbib abs hitind

L50 ANSWER 1 OF 12 HCA COPYRIGHT 2001 ACS
134:106344 Determination of structural and phase parameters of **porous silicon** from capacitance measurements.
Tutov, E. A.; Andryukov, A. Yu.; Kashkarov, V. M. (Voronezh. Gos. Univ., Voronezh, Russia). Zh. Prikl. Khim. (S.-Peterburg, Russ. Fed.), 73(7), 1071-1074 (Russian) 2000. CODEN: ZPKHAB. ISSN: 0044-4618. Publisher: Nauka.
AB **Porous silicon** was prepd. by electrochem. **etching** of single-cryst. n-Si in an aq.-alc. soln. of **HF** in presence of **H2O2** as an oxidizer. The bulk porosity and the effective thickness of oxide phase in **porous Si** were calcd. and the degree of pore coupling was estd.

CC 66-4 (Surface Chemistry and Colloids)
Section cross-reference(s): 76
ST **silicon etching** oxidn **porosity**
capacitance
IT Electric capacitance-potential relationship
Etching
Oxidation
Phase composition
Porosity
(detn. of structural and phase parameters of **porous silicon** from capacitance measurements)
IT 7631-86-9, Silica, formation (nonpreparative)
(detn. of structural and phase parameters of **porous silicon** from capacitance measurements)
IT 7440-21-3, Silicon, properties
(detn. of structural and phase parameters of **porous silicon** from capacitance measurements)
IT **7664-39-3**, **Hydrogen fluoride**, processes
(**etchant**; detn. of structural and phase parameters of **porous silicon** from capacitance measurements)
IT **7722-84-1**, **Hydrogen peroxide**, reactions
(oxidizer; detn. of structural and phase parameters of **porous silicon** from capacitance measurements)

L50 ANSWER 2 OF 12 HCA COPYRIGHT 2001 ACS
133:128756 Separating apparatus, separating method, and method of manufacturing semiconductor substrate using porous layers and liquid injection. Kurisu, Hirokazu; Ohmi, Kazuaki; Yonehara, Takao; Sakaguchi, Kiyofumi; Yanagita, Kazutaka (Canon K. K., Japan). Eur. Pat. Appl. EP 1026727 A2 20000809, 25 pp. DESIGNATED STATES: R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO. (English). CODEN: EPXXDW. APPLICATION: EP 2000-300718 20000131. PRIORITY: JP 1999-25482 19990202.
AB When a bonded substrate stack prepd. by bonding a first substrate in which a single-crystal Si layer is formed on a porous layer, and an insulating layer is formed on the single-crystal Si layer to a 2nd substrate to be sepd. at the porous layer serrate defects at the edge of the sepd. substrates are prevented. A fluid is injected from an injector into the porous layer while rotating the bonded stack around a axis, thereby splitting the stack at the porous layer.
IC ICM H01L021-20
ICS H01L021-762
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 66
IT **Etching**
(selective; sepg. app., sepg. method, and method of manufg. semiconductor substrate using porous layers and liq. injection)
IT **7722-84-1**, **Hydrogen peroxide**, uses
(**etchant** for **porous silicon**; sepg. app., sepg. method, and method of manufg. semiconductor substrate using porous layers and liq. injection)

IT **7664-39-3**, **Hydrogen fluoride**, processes
(sepg. app., sepg. method, and method of manufg. semiconductor substrate using porous layers and liq. injection)

L50 ANSWER 3 OF 12 HCA COPYRIGHT 2001 ACS
131:357614 Blue luminescence from photochemically **etched** silicon. Yamamoto, Naokatsu; Takai, Hiroshi (Tokyo Denki University, Tokyo, 101-8457, Japan). Jpn. J. Appl. Phys., Part 1, 38(10), 5706-5709 (English) 1999. CODEN: JAPNDE. ISSN: 0021-4922. Publisher: Japanese Journal of Applied Physics.
AB Light-emitting layers are formed by the photochem. **etching** of Si in **HF** with **H2O2** as an oxidant under the irradn. of a He-Ne laser (633 nm, 18.4 W/cm2). Photoluminescence (PL) using a He-Cd laser (325 nm) from the **etched** layer has a peak wavelength at 640 nm and a wide full-width at half max. (FWHM) of .apprx.0.3 eV. The peak position and the wide FWHM from the **etched** layer are considered to be similar to those from **porous Si**. The PL peak wavelength can be varied from 700 nm to 640 nm by increasing the **etching** time, so that red or yellow luminescence can be obsd. in daylight. The **etched** layer formed with **H2O2** emits blue photoluminescence at 440 nm after being dipped in an EtOH for 17 h, and the blue light emission can be seen in air. The visible luminescence of the photochem. **etched** layers can be explained by the known quantum size effect of nanocryst. Si.
CC 73-5 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 74
ST blue luminescence photochem **etching** silicon
IT Anodization
Luminescence
Quantum size effect
(blue luminescence from photochem. **etched** and anodized silicon)
IT **Etching**
(photochem.; blue luminescence from photochem. **etched** and anodized silicon)
IT **7664-39-3**, **Hydrogen fluoride**, properties
7697-37-2, Nitric acid, properties **7722-84-1**, **Hydrogen peroxide**, properties
(blue luminescence from photochem. **etched** and anodized silicon)
IT **7440-21-3**, **Silicon**, properties
(**porous**; blue luminescence from photochem. **etched** and anodized silicon)

L50 ANSWER 4 OF 12 HCA COPYRIGHT 2001 ACS
130:358539 Galvanic **porous silicon** formation without external contacts. Ashruf, C. M. A.; French, P. J.; Bressers, P. M. M. C.; Kelly, J. J. (Department of Electrical Engineering, Faculty of Information Technology and Systems, DIMES, Laboratory for Electronic Instrumentation, Delft University of Technology, Delft,

2628 CD, Neth.). Sens. Actuators, A, A74(1-3), 118-122 (English)
1999. CODEN: SAAPEB. ISSN: 0924-4247. Publisher: Elsevier Science
S.A..

AB **Porous silicon** is usually formed under anodic polarization in an electrochem. cell. A technique is described for forming **porous silicon** without using an external current or voltage source. By connecting an inert metal electrode to a silicon sample, both immersed in a **HF** soln., a galvanic cell is formed. Redn. of oxygen at the inert electrode results in the **etching** of Si at the silicon/electrolyte interface. **Porous silicon** is formed at a rate which is dependent on the cell current. The formation rate may be enhanced by adding oxidizing agents to the soln. Galvanic **etching** for forming **porous Si** is a promising alternative for stain **etching** since it gives more uniform and reproducible results.

CC 72-11 (Electrochemistry)
Section cross-reference(s): 52, 66, 76

ST **porous silicon** formation galvanic cell noble metal **hydrofluoric acid**; oxidizing agent **porous silicon** formation galvanic cell **hydrofluoric acid**; oxygen electroredn noble metal galvanic cell **porous silicon** formation

IT Oxidizing agents
(galvanic **porous silicon** formation without external contacts by forming galvanic cell by connecting gold electrode to silicon immersed in **HF** soln. contg.)

IT Electrochemical reduction
(of oxygen at gold or platinum: **porous silicon** formation without external contacts by forming galvanic cell by connecting platinum or gold electrode to silicon immersed in **HF** soln.)

IT Interfacial structure
(of **porous silicon** formed without external contacts by forming galvanic cell by connecting platinum or gold electrode to silicon immersed in **HF** soln.)

IT Electrochemical **etching**
(of **silicon** in **porous silicon** formation without external contacts by forming galvanic cell by connecting platinum or gold electrode to silicon immersed in **HF** soln.)

IT 7782-44-7, Oxygen, properties
(electrochem. redn. at gold or platinum: **porous silicon** formation without external contacts by forming galvanic cell by connecting platinum or gold electrode to silicon immersed in **HF** soln.)

IT 7440-57-5, Gold, uses
(galvanic **porous silicon** formation without external contacts by forming galvanic cell by connecting gold electrode to silicon immersed in **HF** soln.)

IT **7664-39-3**, **Hydrogen fluoride**, uses
(galvanic **porous silicon** formation without

external contacts by forming galvanic cell by connecting noble
metal electrode to silicon immersed in **HF** soln.)
IT 7440-21-3, **Silicon**, properties
(galvanic **porous silicon** formation without
external contacts by forming galvanic cell by connecting noble
metal electrode to silicon immersed in **HF** soln.)
IT **7722-84-1**, **Hydrogen peroxide**, properties
7727-54-0, Ammonium peroxydisulfate
(galvanic **porous silicon** formation without
external contacts by forming galvanic cell by connecting noble
metal electrode to silicon immersed in **HF** soln. contg.)
IT 7440-06-4, Platinum, uses
(galvanic **porous silicon** formation without
external contacts by forming galvanic cell by connecting platinum
electrode to silicon immersed in **HF** soln.)

L50 ANSWER 5 OF 12 HCA COPYRIGHT 2001 ACS
129:75029 **Etching** solution for **etching**
porous silicon, **etching** method using the
etching solution and method of preparing semiconductor
member using the **etching** solution. et al. (Japan). U.S.
US 5767020 A 19980616, 57 pp. (English). CODEN: USXXAM.
APPLICATION: US 1992-835381 19920214. PRIORITY: JP 1991-42212
19910215; JP 1991-42213 19910215; JP 1991-55601 19910228; JP
1991-55602 19910228; JP 1991-55603 19910228; JP 1991-55604 19910228;
JP 1991-55605 19910228; JP 1991-55606 19910228; JP 1991-55607
19910228; JP 1991-55608 19910228; JP 1991-55609 19910228; JP
1991-55610 19910228; JP 1991-55611 19910228; JP 1991-55612 19910228;
JP 1991-55613 19910228; JP 1991-55614 19910228; JP 1991-56603
19910228; JP 1991-85755 19910327; JP 1991-148160 19910524; JP
1991-148161 19910524.
AB A method for prepg. a semiconductor member comprises: forming a
substrate having a non-**porous silicon** monocryst.
layer and a **porous silicon** layer; bonding
another substrate having a surface made of an insulating material to
the surface of the monocryst. layer; and **etching** to remove
the **porous silicon** layer by immersing in an
etching soln.
IC ICM H01L021-20
NCL 438705000
CC 76-3 (Electric Phenomena)
ST **etching** soln **porous silicon** layer
IT Epitaxial films
Etching
(selective **etching** of **porous Si**
layer and non-**porous Si** layer)
IT Epitaxy
Semiconductor device fabrication
(selective **etching** of **porous Si**
layer and non-**porous Si** layer in prepn. of
semiconductor member)
IT 7440-21-3, Silicon, processes

(selective **etching** of **porous Si**
layer and non-**porous Si** layer)
IT **7664-39-3**, **Hydrofluoric acid**, uses
7722-84-1, **Hydrogen peroxide**, uses
12125-01-8, Ammonium fluoride
(selective **etching** of **porous Si**
layer and non-**porous Si** layer with)

L50 ANSWER 6 OF 12 HCA COPYRIGHT 2001 ACS
123:355918 Epitaxial layer transfer by bond and **etch**-back of **porous silicon**. Yonehara, Takao; Sakaguchi, Kiyofumi; Sato, Nobuhiko (Res. Dev. Headquarters, Canon Inc., Hiratsuka, 254, Japan). Proc. - Electrochem. Soc., 95-7(Semiconductor Wafer Bonding: Physics and Applications III), 47-55 (English) 1995. CODEN: PESODO. ISSN: 0161-6374.
AB The authors propose and demonstrate a novel method named ELTRAN for single **etch**-stop bond-and-**etch**-back SOI in which the epitaxial **Si** layers over **porous Si** are transferred onto the dissimilar substrates by **etching** back **porous Si**. The highest **etching** selectivity .apprx.105 is achieved by a soln. of **HF**, **H2O2** and H2O which enables us to fabricate the ultra thin film SOI with excellent active layer thickness variation of less than 7% across 5-in. SOI wafers.
CC 76-3 (Electric Phenomena)
ST epitaxial layer transfer **porous silicon**; bond **etch** back **porous silicon**
IT Epitaxy
Etching
Semiconductor devices
(epitaxial layer transfer by bond and **etch**-back of **porous silicon**)
IT 7440-21-3, Silicon, properties
(epitaxial layer transfer by bond and **etch**-back of **porous silicon**)

L50 ANSWER 7 OF 12 HCA COPYRIGHT 2001 ACS
123:354867 Epitaxial growth on **porous Si** for a new bond and **etchback** silicon-on-insulator. Sato, Nobuhiko; Sakaguchi, Kiyofumi; Yamagata, Kenji; Fujiyama, Yasutomo; Yonehara, Takao (Device Development Center, Canon Incorporated, Kanagawa, 254, Japan). J. Electrochem. Soc., 142(9), 3116-22 (English) 1995. CODEN: JESOAN. ISSN: 0013-4651.
AB A new bond and **etchback** Si-on-insulator (SOI) is proposed and demonstrated, in which epitaxial layers on **porous Si** are transferred by bonding and **etching** back **porous Si**. The key processes are epitaxial growth on **porous Si** and selective removal of **porous Si**. In the epitaxial layers over **porous Si**, the major defects are stacking faults, which can be reduced to 103 to 104/cm2 by raising the H2 prebake temp. and lengthening the immersion time in dild. **HF** prior

to the prebake. Bondable smooth surfaces were formed at growth temps. <900.degree.. A highly selective **etchant** of **HF-H2O2** was discovered and enabled the authors to **etch** off **porous Si** with a selectivity of 105, leaving behind epitaxial layers on the oxidized handle wafers. The rough as-**etched** SOI surface was smooth comparable to that of the com.8 available bulk-polished wafer, and B concn. in the SOI-Si layer was simultaneously decreased to .apprx.1 T 1016/cm3, by H2 annealing. Finally, a uniform SOI layer of 507 nm .+-. 3% across a 5 in wafter was achieved by this method.

CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76

ST epitaxy **porous silicon** bond **etchback** insulator

IT Epitaxy
Semiconductor devices
(epitaxial growth on **porous Si** for a new bond and **etchback** silicon-on-insulator)

IT 7440-21-3, Silicon, processes
(epitaxial growth on **porous Si** for a new bond and **etchback** silicon-on-insulator)

L50 ANSWER 8 OF 12 HCA COPYRIGHT 2001 ACS

122:328450 Manufacturing a semiconductor device capacitor electrode. Toshiyuki, Hirota (NEC Corp., Japan). Eur. Pat. Appl. EP 642155 A1 19950308, 17 pp. DESIGNATED STATES: R: DE, FR, GB. (English). CODEN: EPXXDW. APPLICATION: EP 1994-113762 19940902. PRIORITY: JP 1993-219370 19930903.

AB In manufg. a semiconductor device having a capacitor, the lower electrode of the capacitor is prepd. by forming a polysilicon film contg. a Group V element as an impurity; performing a 1st **etching** step in which an uneven portion is formed on the surface of the polysilicon film by preferably **etching** the more heavily doped crystal grain boundaries; and performing a 2nd **etching** step having an **etch** rate whose impurity concn. dependence is different from that of the **etch** rate of the 1st **etching** step (preferably lower), thus increasing the width of the recessed portions produced by the 1st **etching** step. The 2nd **etching** step also removes **porous Si** left by the 1st **etching** step.

IC ICM H01L021-3205
ICS H01L027-108

CC 76-3 (Electric Phenomena)

IT **Etching**
(in manuf. of semiconductor device capacitor electrodes)

IT 64-19-7, Acetic acid, processes 7664-38-2, Phosphoric acid, processes **7664-39-3**, **Hydrogen fluoride**, processes 7664-41-7, Ammonia, processes 7697-37-2, Nitric acid, processes **7722-84-1**, **Hydrogen peroxide**, processes
(**etching** of polysilicon films for semiconductor device capacitor electrodes by)

L50 ANSWER 9 OF 12 HCA COPYRIGHT 2001 ACS
122:327727 Extremely high selective **etching** of **porous silicon** for single **etch**-stop bond-and-**etch**-back silicon-on-insulator. Sakaguchi, Kiyofumi; Sato, Nobuhiko; Yamagata, Kenji; Fujiyama, Yasutomo; Yonehara, Takao (Device Dep. Cent., Canon Inc., Kanagawa, 254, Japan). Jpn. J. Appl. Phys., Part 1, 34(2B), 842-7 (English) 1995. CODEN: JAPNDE. ISSN: 0021-4922.

AB The **etching** characteristics of **porous Si** in comparison with bulk Si have been investigated for ultrathin film single **etch**-step bond-and-**etch**-back silicon-on-insulator. **Porous Si** can be selectively **etched** exclusively by a mixt. of **HF**, **H2O2**, and H2O due to a structure-sensitive mechanism, i.e., inner reaction by capillary-induced penetration of the **etchant** into the pores followed by collapsing of the Si columns. This extremely high **etching** selectivity reaches as large as 105, which results in excellent SOI layer thickness variation of less than 7% across 5-in. SOI wafers with sub-.mu.m and sub-100-nm thicknesses.

CC 76-3 (Electric Phenomena)

ST selective **etching porous silicon**; **fluoride hydrogen** selective **etching porous silicon**; **hydrogen peroxide** selective **etching porous silicon**

IT Semiconductor devices
(SOI; extremely high selective **etching** of **porous silicon** with **HF/H2O2**/H2O for single **etch**-stop bond-and-**etch**-back SOI)

IT **Etching**
(selective, extremely high selective **etching** of **porous silicon** for single **etch**-stop bond-and-**etch**-back silicon-on-insulator)

IT **7664-39-3**, **Hydrogen fluoride**, reactions
7722-84-1, **Hydrogen peroxide**, reactions
(extremely high selective **etching** of **porous silicon** with **HF/H2O2**/H2O for single **etch**-stop bond-and-**etch**-back SOI)

IT **7440-21-3**, **Silicon**, processes
(**porous**; extremely high selective **etching** of **porous silicon** for single **etch**-stop bond-and-**etch**-back silicon-on-insulator)

L50 ANSWER 10 OF 12 HCA COPYRIGHT 2001 ACS
122:175544 Epitaxial growth on **porous Si** for a new bond and **etch**-back SOI. Sato, Nobuhiko; Sakaguchi, Kiyofumi; Yamagata, Kenji; Fujiyama, Yasutomo; Yonehara, Takao (Semiconductor R & D Center, Canon Inc., Hiratsuka, 254, Japan). Proc. - Electrochem. Soc., 94-10(Semiconductor Silicon/1994), 443-53 (English) 1994. CODEN: PESODO. ISSN: 0161-6374.

AB Selective removal and epitaxial growth on **porous Si** are 2 major processes for a new bond and **etch** -back SOI in which epitaxial layers are transferred by bonding and **etching** back **porous Si**. A highly selective **etchant** of **HF-H2O2** was discovered and enabled one to **etch** off **porous Si** with a selectivity of 105, leaving behind epitaxial layers on the oxidized handle wafers. In epitaxial layers over **porous Si**, the major defects are stacking faults, which can be reduced by increasing H2 prebake temp., and longer immersion in dil. **HF** prior to the prebake. A bondable smooth surface is formed at growth temps. <900.degree.. A low defect d. (104/cm2), and uniform SOI layer of 473 nm .+-.3% across a 5-in. wafer is achieved by this method.

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75

ST epitaxy **porous silicon** bond **etchback** SOI

IT Electric insulators and Dielectrics
Epitaxy
Etching
(epitaxial growth on **porous Si** for a new bond and **etchback** SOI)

IT 7440-21-3, Silicon, processes
(epitaxial growth on **porous Si** for a new bond and **etchback** SOI)

IT **7664-39-3**, **Hydrogen fluoride**, processes
7722-84-1, **Hydrogen peroxide**, processes
(**etching porous Si** by **HF-H2O2** in prepn. of bond and **etchback** SOI)

L50 ANSWER 11 OF 12 HCA COPYRIGHT 2001 ACS

121:266785 Photoluminescence from **porous silicon**.
Nossarzewska-Orlowska, Elzbieta; Brzozowski, Andrzej; Surma, Barbara; Lipinski, Dariusz (Instytut Technologii Materialo Elektronicznych, Warsaw, 01-919, Pol.). Mater. Elektron., 21(4), 28-38, 2 plates (Polish) 1993. CODEN: MAELDK. ISSN: 0209-0058.

AB The results of investigations on prepn. and luminescence properties of **silicon porous** layers are presented. The photoluminescence spectra (PL) were shifted by changing an **HF** concn. used for anodization. Photoluminescence instability is discussed on the basis of the PL and IR absorption (FTIR) spectra from stored in air and intentionally oxidized samples.

CC 73-5 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)
Section cross-reference(s): 72

ST **porous silicon** photoluminescence anodization condition; oxidn **hydrogen peroxide** silicon luminescence

IT Infrared spectra
(for **porous silicon** affected by anodization

conditions and **hydrogen peroxide** oxidn.,
Fourier-transform)
IT Luminescence
(photoluminescence from **porous silicon**
affected by anodization conditions and oxidn. in **hydrogen**
peroxide)
IT Oxidation
(photoluminescence from **porous silicon**
affected by **hydrogen peroxide** oxidn.)
IT **Etching**
(electrochem., photoluminescence from **porous**
silicon affected by)
IT 7440-21-3, Silicon, properties
(photoluminescence from **porous silicon**
affected by anodization conditions and oxidn. in **hydrogen**
peroxide)
IT **7664-39-3**, **Hydrofluoric acid**, uses
(photoluminescence from **porous silicon**
affected by anodization in soln. contg.)
IT **7722-84-1**, **Hydrogen peroxide**, processes
(photoluminescence from **porous silicon**
affected by oxidn. by)

L50 ANSWER 12 OF 12 HCA COPYRIGHT 2001 ACS
107:107186 Microfabrication of molecular scale microstructures.
Deckman, H. W.; Abeles, B.; Dunsmuir, J. H.; Roxlo, C. B. (Exxon
Res. and Eng. Co., Annandale, NJ, 08801, USA). Appl. Phys. Lett.,
50(9), 504-6 (English) 1987. CODEN: APPLAB. ISSN: 0003-6951.
AB Microfabrication techniques were used to prep. a new class of mol.
scale microporous materials. These materials are formed by chem.
etching slots into alternate layers of a lithog. exposed
amorphous superlattice cross section. The slot width is accurately
controllable from 10 .ANG. to more than 500 .ANG..
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 66, 74
ST mol scale microporous material fabrication; chem **etching**
microporous material fabrication; superlattice amorphous chem
etching microporosity
IT Semiconductor devices
(**etching** in fabrication of, with superlattice
structure)
IT **Etching**
(of amorphous superlattice cross sections, in manufg. of
microporous materials)
IT Porous materials and Cellular materials
(micro-, prodn. of, by chem. **etching** of amorphous
superlattices)
IT **7664-39-3**, **Hydrogen fluoride**, reactions
7722-84-1, **Hydrogen peroxide**, reactions
13709-36-9, Xenon difluoride
(**etching** by, in prodn. of microporous material from
superlattices)

IT 11126-22-0, Silicon oxide 12033-89-5, Silicon nitride, properties
(superlattices of amorphous hydrogenated **silicon** with, in **microporous** material fabrication by chem. **etching**)

IT 1333-74-0, Hydrogen, uses and miscellaneous
(superlattices of amorphous silicon contg., with silicon oxide or silicon nitride or germanium, in microporous materials fabrication by chem. **etching**)

IT 7440-21-3, Silicon, uses and miscellaneous
(superlattices of silicon oxide or silicon nitride with amorphous hydrogenated, for microporous material fabrication by chem. **etching**)